eWLB
Embedded Wafer Level Ball Grid Array

We offer customers a high performance fan-out wafer level packaging (FOWLP) solution that provides significant bandwidth, performance, form factor and cost benefits compared to other packaging technologies available today.

Proven Leadership
- Versatile platform for advanced system level integration
- Highest integration density commercially available in the industry today
- Flexibility to integrate die from diverse processes, manufacturing sources & silicon wafer nodes for increased functionality
- Excellent mechanical, electrical & thermal performance
- Effectively accommodates new lithography nodes
- Flexible, cost effective 2D, 2.5D & 3D solutions across a broad range of market segments & applications

Features
Performance
- Unprecedented flexibility in 2.5D & 3D integration with Si partitioning capabilities
- Advanced dielectric materials for highly reliable, power-efficient solutions
- Strong electrical performance (capable to beyond 80GHz) and fit for mmWave/5G devices
- Highly effective heat dissipation for strong thermal performance
- KGD process helps achieve strong yields (99.9%)
Application Space
When determining the optimal platform among the space of device I/O densities and product architectures, early stage co-design helps ensure the lowest cost solution. As the gap between chip I/O and PCB density increases, we have analyzed the fan-out ratio of different package designs and identified the "sweet spot" for eWLB.

Component Level Reliability

| Moisture Sensitivity Level | MSL1 @ lead free condition (260°C) |
| Temperature Cycling (after precon) | -55°C/125°C, 1000 cycles |
| Unbiased HAST | 130°C/85% RH, 96 hrs |
| High Temperature Storage | 150°C, 1000 hrs |
| Temperature Humidity Bias Test | 85°C/85%/5V, 1000 hrs |
| High Temperature Operating Life | JESD22-A109, 125°C, 1000 hrs |
| Multiple Solder Reflow | 5x, 10x and 20x refows with minimal reduction in bump shear strength |

Board Level Reliability

| Temperature Cycling on Board | -40°C/125°C, 2 cycles/hr, 500 cycles |
| Drop Test | Passed JEDEC drop test for 8 x 8mm, 183 balls (0.5mm pitch) |
| Bend Test | Passed JEDEC bend test, 300 cycles |
| Temperature Humidity Bias Test | 85°C/85%, RH, 5V, 1000 hrs (performed mounted on PCB) |

Thermal Performance $\theta_{ja}$ (°C/W)
Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

<table>
<thead>
<tr>
<th>Body Size</th>
<th>Die Size</th>
<th>Thermal Performance $\theta_{ja}$(°C/W)</th>
<th>Thermal Vias (on test board)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 x 8mm</td>
<td>5 x 5mm</td>
<td>32.5</td>
<td>simulation data</td>
</tr>
<tr>
<td>12 x 12mm</td>
<td>8 x 8mm</td>
<td>21.7</td>
<td>simulation data</td>
</tr>
<tr>
<td>14 x 14mm</td>
<td>10 x 10mm</td>
<td>17.7</td>
<td>simulation data</td>
</tr>
</tbody>
</table>

Notes: Thermal performance in the 15-35°C/W range without thermal enhancement. Application specific thermal characterization available upon request.

eWLB Process Flow
1. Reconstituted wafer
   - Wafer saw and pick-and-place from incoming wafer
   - Probed good die
   - Molded reconstituted wafer using proven materials
   - Molded artificial wafer starting point for thin film technology
2. Redistribution
   - Thin film technology with advanced design rules
   - Standard thin film equipment
   - Proven and reliable material set
3. Ball Mount and Singulation
   - Standard back-end assembly flow (and equipment)

Specifications
- Body sizes: 2 x 2mm to 15 x 15mm in high volume production; up to 16 x 16mm qualified
- Bump Pitch: 0.3mm minimum
- Bump Height: 0.16mm/0.2mm / 0.23mm (0.35mm / 0.4mm /0.5mm pitch)
- Backside Coating: Laminated coating (optional)
- Marking: Laser marking
- Inspection: Automatic optical inspection w/ electronic wafer mapping
- Packing Options: Fully automated die pick/place into custom pocket tape/reel or waffle pack media

eWLB Products Portfolio
- The most comprehensive FOWLP portfolio in the industry
- Wide range of small die, large die, flip chip, stacked or side-by-side multi-die & ultra-thin options
- Body sizes: 2 x 2mm – 15 x 15mm in high volume manufacturing and qualified up to 16 x 16mm
- 2D solutions in single & multi-die configurations down to 0.3mm height
- 2.5D solutions in single & multi-die configurations down to 0.3mm height
- 3D eWLB interposer solutions (replaces stacked package configurations or to enable 3D TSV)
- 3D SiP & PoP solutions include embedded multiple heterogenous passives & active components, face-to-back or face-to-face options & single-sided, 1.5 & double-sided PoP (total stacked PoP height <1.0mm) & SiP configurations
- MCP versions with flip chip, discrete, crystal & IPD integration capability