

FBGA-SD

Fine Pitch Ball Grid Array - Stacked Die

Highlights

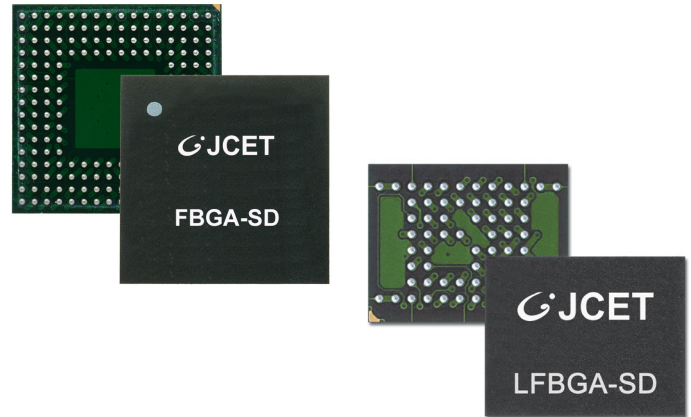
- Laminate substrate-based package enabling 2, 3 and 4 layers of routing flexibility
- Available in 1.4mm to 1.7mm (LFBGA-SD), 1.2mm (TFBGA-SD), 1.0mm (VFBGA-SD), 0.80mm (WFBGA-SD) and 0.65mm (UFBGA-SD) maximum package thickness
- Stacking of die allows for more functionality in an array molded, cost effective, space saving package solution

Features

- 2 die to 7 die stack with spacer capability
- 4 x 4mm to 23 x 23mm body size
- Package height at 0.65, 0.80, 1.0, 1.2, 1.4 and 1.7mm max.
- Flexible die stacking options (pyramid, same die, etc.)
- 0.4mm to 1.0mm ball pitch; eutectic and Pb-free solder ball; smaller ball size for reduced height
- Memory, Logic, Analog and RF device combinations
- JEDEC standard package outlines
- Die thinning down to 40µm
- Low loop wire bonding; reverse and die to die
- Up to 2mm die overhang per side
- Halogen-free and low-K wafer compatible BOM
- Film spacer capability for decreased die stack thickness
- Very thin substrate capability
- Capability to integrate discrete passives or integrated passive devices
- Very thin substrate capability

Applications

- Suitable for a variety of applications including memory integration
- Chipset integration (Analog/Digital), mixed technologies integration (Baseband/RF)
- Handheld products (Cellular Phones, Gaming, MP3 Players, GPS)
- Consumer electronics (Internet applications, Digital Cameras/ Camcorders)
- Other applications requiring device integration in minimal form factors



Description

Fine Pitch Ball Grid Array (FBGA) is a laminate substrate-based chip scale package with plastic overmolded encapsulation and an array of fine pitch solder ball terminals. FBGA is a package that is widely used in space constrained applications such as mobile and handheld computing devices. FBGA's reduced outline and thickness and higher density options make it an ideal advanced technology packaging solution for high performance and/or portable applications.

Our Fine Pitch Ball Grid Array Stacked Die (FBGA-SD) offering includes LFBGA-SD, TFBGA-SD, VFBGA-SD, WFBGA-SD and UFBGA-SD packages. Our chip stack technology offers the flexibility of stacking 2 to 7 die in a single package. Die to die bonding capability enables device and signal integration to improve electrical performance and reduce overall package I/O requirements. Wafer thinning technology, overhang wire bond technology and the use of spacers between stacked die provide the flexibility to stack almost any desirable configuration of die in one package. This capability uses existing assembly infrastructure, which results in more functional integration with lower overall package cost.

The use of the latest packaging materials allows this package to meet JEDEC Moisture Resistance Test Level 2A with lead-free reflow conditions. This is an ideal package for integrating memory for mobile phones. It is also used to integrate logic and memory, logic and analog, or combinations of memory, logic, analog and RF.



Specifications

Die Thickness	40 - 165µm (1.6 - 6.5mils)
Mold Cap Thickness	0.3 - 1.0mm
Marking	Laser
Packing Options	JEDEC tray/tape & reel

Reliability

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (-65°C to 150°C), 1000 cycles
High Temperature Storage	150°C, 1000 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

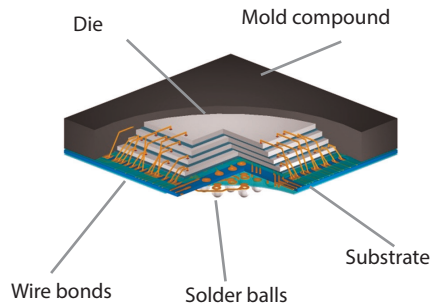
Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	34 - 119	1.30 - 4.55	0.26 - 2.28	0.25 - 0.95	0.06 - 0.42
Total (2L)	4 - 9	154 - 239	2.95 - 6.20	0.71 - 3.13	0.35 - 1.05	0.07 - 0.44
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	34 - 119	0.90 - 3.15	0.18 - 1.58	0.35 - 1.10	0.06 - 0.42
Total (4L)	4 - 9	154 - 239	2.55 - 4.80	0.63 - 2.43	0.45 - 1.20	0.07 - 0.44

Note: Net = Total Trace Length + Via + Solder Ball.

Cross Sections



Package Configurations

Package Type	Package Thickness Typical (mm)	Body Size (mm)	Ball Count	Ball Pitch (mm)
LFBGA-SD	1.7, 1.4 max	Range: 4x4~23x23	16-700	0.4-0.1
TFBGA-SD	1.2 max	Common sizes: 5x10,		
VFBGA-SD	1.0 max	7x9, 8x8, 8x10, 8x11,		
WFBGA-SD	0.8 max	8x14, 10x10, 10x12,		
UFBGA-SD	0.65 max	10x14, 12x12, 13x13, 15x15, 16x16, 17x17		

