

# Innovations in Wafer Level Technology

## A proven leader in Wafer Level Packaging technology

The demand for breakthrough performance has driven integration technology to new levels of complexity in semiconductor package designs. The need for compact, high performance semiconductor packages is challenging traditional packaging technology in the areas of form factor, reliability and performance. Integration is increasingly moving from substrate-based package configurations to wafer level package designs.

As die sizes and lithography nodes shrink, the JCET Group of companies is driving a number of integration solutions in wafer level packaging, including Fan-in Wafer Level Packaging (FIWLP), Fan-out Wafer Level Packaging (FOWLP), System-in-Package (SiP), Ultra Fine-Pitch Organic Substrate (uFOS), Through Silicon Via (TSV) and Integrated Passive Devices (IPD).

If your end-market application requires a compact, high performance solution with proven reliability and design flexibility, we offer a full range of advanced wafer level technology solutions to help you meet your business goals.



## Fan-in WLP: Compact Packaging Solution

As a small, lightweight, high performance semiconductor solution, Wafer Level Chip Scale Packaging (WLCSP) is a Fan-in wafer level package (WLP) that offers compelling advantages for cost and space constrained mobile devices and new applications such as wearables and automotive electronics.

With WLCSP, all of the manufacturing process steps are performed in parallel at the silicon wafer level rather than sequentially on individual chips to achieve a package that is essentially the same size as the die.

The basic structure of WLCSP comprises an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides. The WLCSP provides the smallest possible package size since the final package is no larger than the die itself. WLCSP solutions provide significant

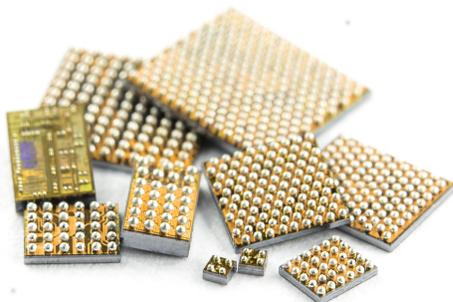
package footprint reductions, lower cost, improved electrical performance, and a relatively simpler construction over conventional wirebond or interposer packaging technologies.

The volume of WLCSP packages used in the industry has experienced steady growth driven by the small form factor and high performance requirements of mobile and consumer products.

### Encapsulation for Increased Reliability

Since WLCSP is essentially a bare die with exposed Si surfaces, there is always risk the package may suffer mechanical damage in the form of chipping and cracking in the course of processing and shipping or during surface mount technology (SMT) operations.

Customers with robust reliability requirements have the option of encapsulating the back and four sidewalls of the die. This provides mechanical robustness and resistance to chipping, cracking and handling damage, enabling improved long term reliability over traditional bare die WLCSP. Encapsulation also provides significant structural protection for advanced node products where the die is very thin and dielectric layers are extremely fragile.



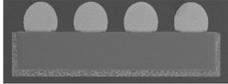
## eWLCSP™ and FI-ECP

We offer two types of Fan-in WLP with protective sidewall coating – encapsulated Wafer Level Chip Scale Packaging (eWLCSP) and Fan-in Encapsulated Chip Package (FI-ECP).

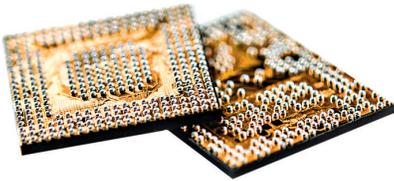
With eWLCSP, the formation of a protective polymer coating on the back and four sides of the die surfaces is accomplished using the same high volume reconstitution and wafer level molding process that is used for our Fan-out embedded Wafer Level Ball Grid Array (eWLB) technology.

FI-ECP has a similar package structure, but follows a different manufacturing flow based on plasma dicing and the lamination process.

If your application requires body sizes below 3x3mm and very thin silicon die, FI-ECP will provide a robust solution to meet your needs. For body sizes above 3x3mm and standard die thicknesses, eWLCSP will provide the best solution.

eWLCSP	FI-ECP
Large body size (>3x3mm)	Smaller body size (<3x3mm)
Standard Si die thickness (350 - 400µm)	Very thin Si die (100 - 150µm)
Reconstitution and wafer level molding process similar to Fan-out Wafer Level Packaging	Plasma dicing and lamination process
	

## Fan-out WLP: High Performance, High Density Solution



Fan-out Wafer Level Packaging (FOWLP) is an advanced packaging technology platform that provides a high density interconnection, superior electrical performance

and the ability to integrate multiple heterogeneous dies in a cost effective, low-profile semiconductor package.

The fan-out structure enables the interconnects to be routed to the outside of the die, thus reducing the amount of silicon real estate needed to accommodate very high input/output (I/O) densities.

By eliminating the discrete chip-to-package interconnect that typically requires a flip chip bump or wirebond, FOWLP

delivers measurable advantages in cost, reliability and performance.

FOWLP devices are manufactured with a chip-first or a chip-last process flow. Chip-first has been in volume production for close to a decade, with yields that are comparable to other packaging technologies. Chip-last is a new approach that has been developed as an option for high performance 2.5D and 3D multi-die package integration.

The JCET Group offers customers both chip-first and chip-last FOWLP technology to meet specific business requirements. Our chip-first solutions are embedded Wafer Level Ball Grid Array (eWLB) and Fan-out Encapsulated Chip Package (FO-ECP). Each FOWLP solution addresses specific areas of need for our customers.

eWLB	FO-ECP
High performance FOWLP	Mid performance FOWLP
300mm/HD panel size	200mm panel size
Best solution for mid to large body sizes with >200 I/O	Best solution for smaller body sizes with lower I/O (~100)
Below 10/10µm line width/line space	Above 10/10µm line width/line space
Multiple redistribution layers (RDL)	Low profile with overmold structure (100 - 150µm die thickness)
Heterogeneous integration in 2.5D, 3D, Package-on-Package (PoP) and System-in-Package (SiP)	LGA, BGA and multi-chip packages



## eWLB

Embedded Wafer Level Ball Grid Array (eWLB) is one of the most widely adopted FOWLP solutions in the semiconductor industry today. eWLB provides a significant increase in routing density combined with an unparalleled reduction in package size and thickness which is not attainable with substrate-based packages. The smaller form factor helps to free up space on the circuit board. The short interconnection lengths combined with thinner dielectric materials also produce better electrical performance with a significant reduction in power consumption, thereby improving battery life.

JCET, was one of the first companies to ramp eWLB to high volume production over 9 years ago and has driven a number of industry-wide technology achievements such as dense vertical interconnections as high as 500 – 1,000 I/O, very fine line and widths spacing down to 2µm/2µm, ultra-thin package profiles, and multiple redistribution layers (RDL).

### 2.5D / 3D eWLB Integration

The integration capabilities and design flexibility of eWLB is driving adoption in a number of emerging market segments such as Internet of Things (IoT), wearable electronics such as health bands and cardiac monitoring devices, fingerprint sensors, MEMS, 5G mmWave devices, and automotive applications such as Advanced Driver Assistance Systems (ADAS). If the end application requires a reduction in form factor and thinner package with a high level of integration and robust reliability, eWLB can provide a superior solution.

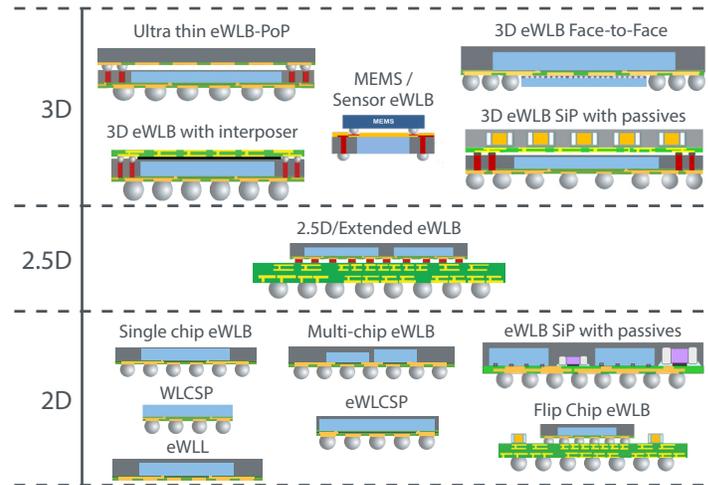


We have developed comprehensive capabilities, including design rules, advanced packaging technologies, high density SMT component placement, advanced molding for complex topographies, conformal shielding, and system level test to deliver highly integrated 2.5D and 3D eWLB solutions.

Our 2.5D eWLB interposers can connect one active die to another, enabling very dense interconnection with more effective heat dissipation, improved processing speed and the flexibility to integrate die from different manufacturing sources. The result is a proven 2.5D solution that is superior to Through Silicon Via (TSV) in terms of overall cost effectiveness and process simplicity.

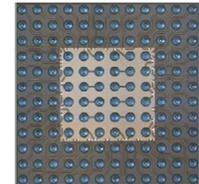
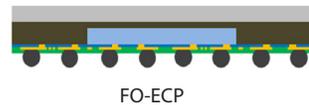
Our 3D System-in-Package (SiP) and Package-on-Package (PoP) solutions include embedded multiple passives and active components, face-to-back or face-to-face options, and single-sided, 1.5-sided and double-sided ultra-thin PoP configurations. For applications requiring full 3D integration, our face-to-face eWLB PoP configuration provides a direct vertical interconnection between an application processor die and a memory die through the eWLB mold layer to enable a high bandwidth, very fine pitch structure with performance that parallels TSV technology.

Our extensive eWLB portfolio includes small die, large die, side-by-side multi-die, MEMS, 2.5D and 3D Package-on-Package (PoP) and System-in-Package (SiP) architectures.



### Fan-out Encapsulated Chip Package

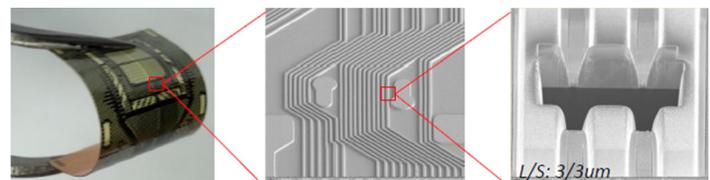
Fan-out Encapsulated Chip Package (FO-ECP) is a newly developed FOWLP with the flexibility to handle various types of thin packaging requirements. FO-ECP is an effective solution for smaller body sizes and features a low profile over-mold structure with 100-150µm thin die.



### Ultra Fine Pitch Organic Substrate

Ultra Fine-Pitch Organic Substrate (uFOS) is an innovative technology for high density devices with LW/LS requirements down to 2/2µm and multiple redistribution layers (>10) in a thin, flexible structure. The versatile uFOS technology features a Cu RDL/ polyimide-based film substrate, substrate insert, or interposer that achieves a high density packaging platform for silicon integration.

uFOS meets the requirements of next generation application processor to memory interconnects in high performance markets. uFOS provides chip-last FOWLP solutions with a flip chip attachment on ultra fine, multi-layer RDL panels. It also creates a cost-effective alternative for 2.5D TSV technology, particularly when used in a 2.5D FOWLP solution or 2.1D organic interposer. Potential applications are FPGA (die partition), memory (Wide I/O, HBM, HMC), networking (photonic) and high performance graphics.



## Through Silicon Via (TSV)

Through Silicon Via (TSV) utilizes short vertical interconnections or “vias” that pass through a silicon wafer in order to achieve greater space efficiencies and higher interconnect densities than wire bonding and flip chip stacking. When combined with microbump bonding and advanced flip chip technology, TSV technology provides the ability to scale semiconductor devices to smaller and smaller geometries with higher input/output.

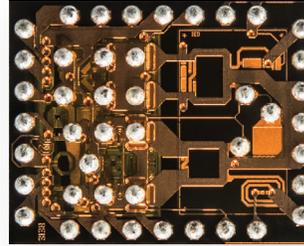
We understand the cost and supply chain limitations our customers face with utilizing TSV technology. The JCET Group is focused on providing customers with cost effective TSV solutions in key areas.

For over two years JCET has been in volume production of 3D TSV for 200mm CMOS Image Sensor (CIS) wafers. The tapered via utilizes a via-last approach to contact the die pad from the wafer backside. This proven approach is also a good fit for other sensor applications such as fingerprint sensors (FPS) or pressure sensors.

For 3D integrated circuits, JCET has a full front- to back-end manufacturing capabilities and currently handles both chip-to-chip (C2C) and chip-to-wafer (C2W) assembly for 3D TSV technology. This includes high density microbump capabilities in both solder and copper column, microbump bonding down to 40µm pitch, thin wafer handling, wafer-level underfill, thin

wafer dicing and microbumps for flip chip interconnection. Microbump technology is critical to delivering fine pitch, low profile solutions for high performance devices.

## Integrated Passive Devices (IPD)



Passive devices such as resistors, capacitors, inductors, filters and baluns can consume 60-70% of available space in a system, subsystem or SiP. As one of the first companies in the industry to integrate and fabricate passive devices at the silicon wafer level, we are able

to produce IPDs which are significantly smaller, thinner and higher performing than standard discrete passive devices that are commercially available today.

With this knowledge and experience, we have embedded passive devices in very close proximity to the active die, providing significant performance, size reduction and device integration in SiP configurations that address 2.5D and 3D integration requirements.