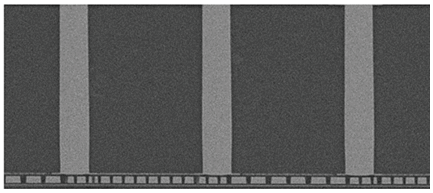
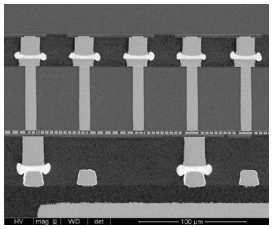
TSV

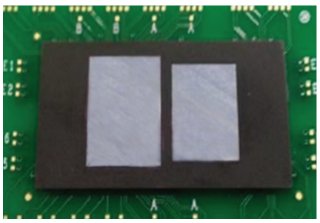
Through Silicon Via



Through Silicon Via



3D TSV Interconnect



Multi-die Integration

Highlights

- Enabling 2.5/3D package for low power, high performance devices in the the graphic, networking and AI markets
- Key requirement in the convergence of high functionality at the lowest energy/performance metric with High bandwidth memory (HBM) and 3D MEMS/Sensor
- Higher interconnect density and greater space efficiencies compared with traditional wirebonding and flip chip stacking by means of face-to-back and face-to-face bonding

TSV Capabilities

TSV Assembly/Packaging (BEOL)

- Chip-to-Wafer or Chip-to-Chip attachment options
- Fine pitch microbump bonding (solder, Cu pillar) and stealth dicing
- Wafer level underfill (ultra small gap underfill process)
- TSV package reliability and characterization
- Developing Next-Generation 2.5/3D TSV packaging

TSV Post-Process (MEOL)

- Bumped wafer thinning and planarization
- Temp bonding/de-bonding
- Backside via reveal
- Dielectric deposition
- Silicon recess and backside metallization
- Thin wafer with TSV handling and dicing
- Microbump technology for 40μm bump pitch plating

TSV Silicon Interposer Technology

- First step for TSV integration
- Qualified tapered TSV process for low density Si interposer (sub-200μm pitch)
- High density Si interposer with TSV in joint development
- Potential to replace high-end organic (BU) substrates
- Thinner profile, tighter pitch and high thermal/electrical performance

Overview

TSV is an important developing technology that utilizes short vertical interconnections or "vias" that pass through a silicon wafer in order to achieve greater space efficiencies and higher interconnect densities than wire bonding and flip chip stacking. When combined with microbump bonding and advanced flip chip technology, TSV provides the ability to scale semiconductor devices to smaller and smaller geometries with higher input/output. We offer complete TSV capabilities covering Mid-end-of-Line (MEOL) processes through Back-end-of-Line (BEOL) assembly and test.

2.5 and 3D Integration with TSV

The need for higher levels of integration, improved electrical performance, reduced power consumption, faster speed, smaller device sizes and shorter interconnects is driving a shift to more complex 2.5D and 3D package designs utilizing TSV technology.

2.5D Integration

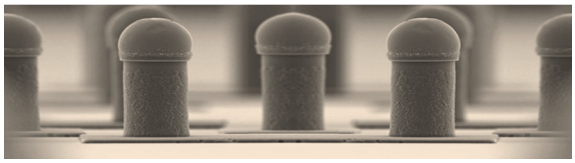
One of the first implementations of TSV technology is in the form of silicon interposers used to bridge 2D silicon designs into more advanced and efficient 3D configurations. TSV interposers provide the flexibility for the integration of die from different technology nodes and deliver advantages in miniaturization, thermal performance and fine line/width spacing in a semiconductor package.

3D Integration

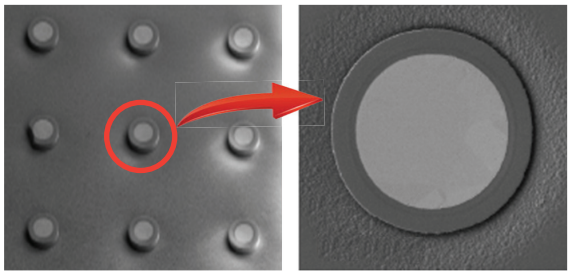
3D ICs can achieve higher bandwidths and performance with TSV, delivering more functionality in a smaller footprint for application processors, image sensors, logic, DRAM, analog, RF flash and MEMS. 3D ICs also provide the platform to integrate different wafer nodes such as 28nm for high speed logic and 130nm for analog within a single package. 3D ICs with TSV are expected to benefit areas such as networking, graphics, artificial intelligence (AI), data center and computing, especially for applications that require ultra-light, small and low-power devices such as multi-core CPUs, GPUs, smartphones and wearable Internet of Things (IoT) products.

TSV Mid-End Fabrication (MEOL)

The mid-end TSV process flow occurs between the wafer fabrication and back-end assembly process and supports the advanced manufacturing of 2.5D and 3D packaging, including wafer level, flip chip and embedded die technologies. Our MEOL assembly services include microbump technology, temporary bonding/de-bonding, wafer thinning and planarization, backside via reveal, isolation and metallisation. Microbump is required to meet fine pitch, low profile applications in 3D TSV stacking and assembly.



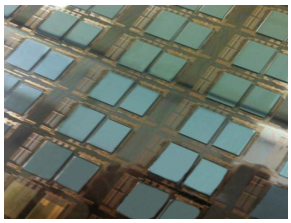
Microbump



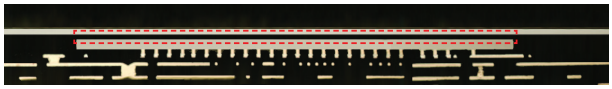
10µm diameter Cu TSV reveal after thinning and CMP

TSV Back-End Capabilities (BEOL)

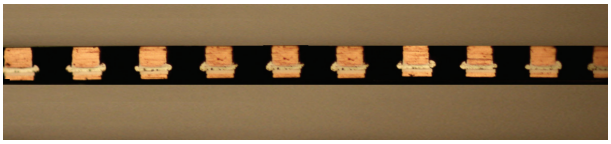
We were one of the first OSAT providers to invest in back-end of line manufacturing capabilities for 2.5D and 3D TSV technology. Our BEOL services include chip-to-chip (C2C) and chip-to-wafer (C2W) assembly, high density microbump capabilities in both solder and copper column, ultra fine pitch microbump bonding, thin wafer handling, wafer level underfill, thin wafer dicing and microbump for flip chip interconnection. Microbump technology is critical to delivering fine pitch, low profile solutions for high performance devices.



3D stacked TSV

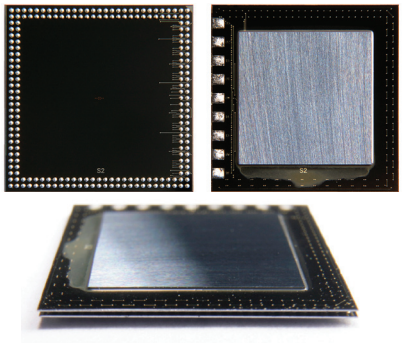


fcFBGA with thermal compression bonded microbumps on the TSVs

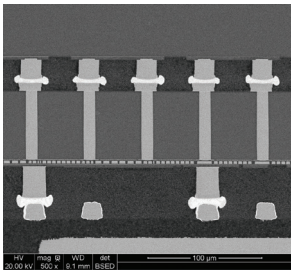


TSV Interposer and Assembly

We offer TSV interposer fabrication to provide a "bridge" between today's 2D packaging solutions and next-generation 3D technology. Often referred to as 2.5D technology, TSV interposers are an efficient and practical approach to die level integration. TSV interposers provide flexibility for the integration of die from different technology nodes and deliver advantages in miniaturization, thermal performance and fine line/width spacing in a semiconductor package.



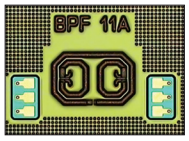
TSV Technology Integration

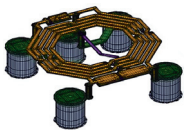


We are able to incorporate TSV and Integrated Passive Devices (IPD) technologies with embedded Wafer Level Ball Grid Array (eWLB) technology in advanced 2.5D and 3D designs to effectively address heterogeneous technology integration where mixed die sizes and silicon lithography nodes are combined into thin package profiles to meet enhanced flexibility, functionality and form factor objectives.

Benefits of TSV in IPD

- Adding TSV to the IPD structure results in a unique high functionality solution
- Performance and margin improvements result from increased distance between IPD surface and ground plane





GSM Balun IPD with TSV

JCET Group Co., Ltd.
www.jcetglobal.com