Flip Chip BGA

fcBGA, fcBGA-SiP, fcBGA-H, fcBGA-MCM

Highlights

- High performance, low cost packages
- Superior thermal solutions
- Package options ranging from bare die, stiffener only, and one/two piece heat spreader
- ABF buildup to 7-2-7; core thickness down to 200µm; coreless substrate and grounded lid for high electrical performance
- Green flip chip solution with Pb-free, Cu pillar bump and halogen-free, low alpha, material sets

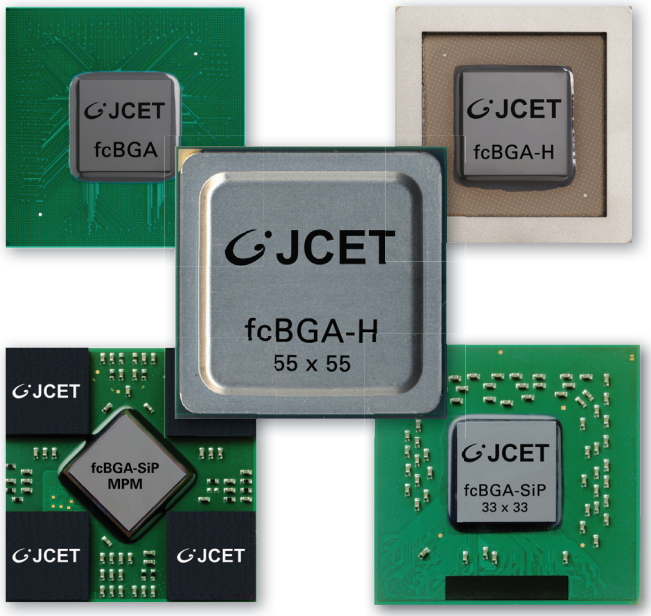
Features

- Body sizes qualified from 12mm x 12mm to 60mm x 60mm, and 67.5 X 67.5mm in development
- Pb-free, and Cu pillar (Cu pillar micro bumps qualified)
- Cu pillar with Mass Reflow (MR) and Thermo compression bonding (TCB)
- Bump pitch qualified: 130µm for Pb-free; 80µm for Cu pillar
- 0.5mm BGA pitch
- 40/32/28/20/16nm Si nodes qualified and 7nm in development
- Nitride, Polyimide, PBO wafer passivations qualified & in production
- Ni-Au, Ni-Pd-Au, solder-on-pad (SOP), OSP organic solderable preservative (OSP) and immersion Sn finish
- Bumped wafer thinning down to 100mm for non-molded fcBGA
- 300mm (plated) bumped wafers; RDL with 200mm and 300mm bumped wafers
- Seamless integration of flip chip, SMT and in-line open/short testing operations
- F/A metrology tools for rapid diagnostics and debugging, including TDR, CSAM, X-ray, Ion milling and SEM
- All packages qualified to JEDEC specifications and/or custom requirements based on end applications (including Automotive grade)

Applications

We offer a complete fcBGA portfolio of high to low-end packages for the Network, Computing, Gaming, Artificial Intelligence (AI), Automotive, and Consumer markets.

- Networking solutions (ASIC, ASSP, Logic, FPGA, and others) for small cell base stations, network storage driven by Cloud computing and high speed/bandwidth Ethernet/network processors
- Computing solutions for DDR4/5 Memory/Datacenter CPU, hybrid/Tablet APU, Graphics Processing Units (GPU), HDD storage migrating to flip chip, HDD/memory market
- Consumer solutions for DTVs, STBs , Game Consoles and the IOT (Smart wired home)



Flip Chip Ball Grid Array packages (fcBGA) form a subgroup of the Flip Chip package family. The fcBGA package is the main platform in this sub-group, which also includes bare die, stiffener only and a thermally enhanced version with one/two piece heat spreader or lid (fcBGA-H), System-in-Package (fcBGA-SiP) versions and a package subsystem meeting the standard BGA footprint that contains multiple components within the same package (fcBGA-MPM). Options also include configurations with thin core, Pb-free and copper pillar bumps. Our Flip Chip BGA packages are available in ball counts ranging from 220 to 4000+, body sizes from 12 x 12mm to 60 x 60mm.

We offer a complete fcBGA portfolio for the network, computing, gaming, artificial intelligence, automotive, and consumer markets. Demand for greater functionality and significantly higher processing speeds in consumer and networking devices is driving flip chip technology to provide cost effective, scalable packages with ultra low K dielectrics, high power integrity, superior thermal performance and higher resistance to electromigration (EM) in very large package sizes, with very fine bump pitches Cu pillar and lead-free solder.

Flip chip interconnection provides the ultimate in miniaturization, reduced package parasitics and enables new paradigms in the area of power and ground distribution to the chip not feasible with other traditional packaging approaches. Our full turnkey services range from design through production, including high speed, high pin count digital and RF testing.

Specifications

Die Thickness	100mm - 760mm
Bump Pitch	Minimum 130µm area array (Pb-free) and 80µm (Cu pillar)
Marking	Laser
Packing Options	JEDEC tray

Reliability

Moisture Sensitivity Level	JEDEC Level 4 or 3 (peak temp 230°, 245° or 260°C)
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiasted HAST	130°C, 85% RH, 96 hrs (typical)

Thermal Performance

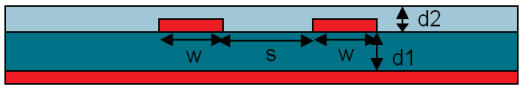
Body Size (mm)	Ball Count	Die Size (mm)	θjc (°C/W)	Natural Convection	θja (C/W) 1 m/s	θja (C/W) 2 m/s
31	792	9.6	1.1	14.0 / 10.0"	11.8 / 6.0"	11.0 / 5.7"
35	964	11.1	0.8	12.5 / 8.9"	11.0 / 5.5"	10.0 / 5.2"
40	1417	15.1	0.4	10.7 / 7.6"	8.7 / 4.3"	7.7 / 4.0"
45	1732	17.4	0.3	9.0 / 6.5"	7.5 / 3.9"	6.5 / 3.5"
55	3213	20.0				
60	3477	25.0				
67.5	4344	33.0				

Notes: *Includes heat sink (0.5" tall, channel design). Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2 or forced convection defined in JESD51-6.6.0".

Electrical Performance

Parametric Data: Sample Embedded Micro-Stripline Configuration

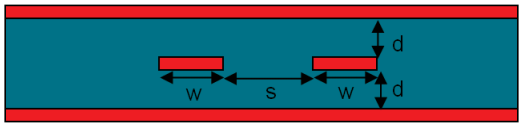
Metal Thickness	Prepreg Thickness (d1)	Solder Mask Thickness (d2)	Trace Width (w)	Trace Spacing (s)	Inductance (nH/mm)	Capacitance (pF/mm)	Ind. Trace Lossy Z11@1GH	Diff. Pair Lossy Z11@1GH	Lossy Propogation Delay Even Mode	Odd Mode
15µm	40µm	35µm	25µm	25µm	0.408	0.109	69.9WΩ	84.1WΩ	6.10ps/mm	6.54ps/mm
				40µm	0.414	0.097	70.9WΩ	100.4WΩ	6.12ps/mm	6.39ps/mm



Conductor material = copper
Prepreg material dialetric constant = 3.4@1GHz
Solder mask material dielectric constant = 3.9@1GHz

Parametric Data: Sample Stripline Configuration

Metal Thickness	Prepreg Thickness (d)	Trace Width (w)	Trace Spacing (s)	Inductance (nH/mm)	Capacitance (pF/mm)	Ind. Trace Lossy Z11@1GH	Diff. Pair Lossy Z11@1GH	Lossy Propogation Delay Even Mode	Odd Mode
15µm	40µm	35µm	25µm	0.323	0.126	54.6WΩ	81.6WΩ	6.37ps/mm	6.46ps/mm
			50µm	0.329	0.117	55.5WΩ	99.0WΩ	6.38ps/mm	6.40ps/mm



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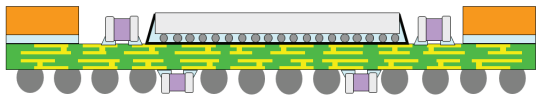
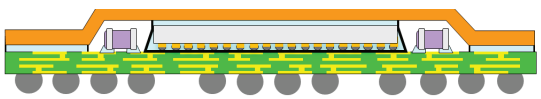
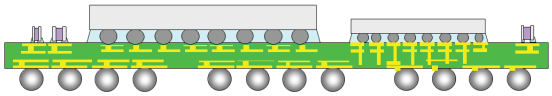
Cross Sections



fcBGA with stiffener



fcBGA-H with Cu pillar



fcBGA-MCM-SiP

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