Fan-in PoP

Fan-in Package-on-Package: : V/TFBGA-FiPoPb-SDx/SDx+y, U/W/V/TFBGA-SDx

Highlights

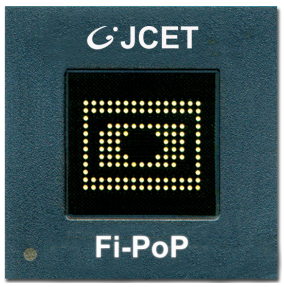
- Stacking fully tested memory and logic packages eliminates known good die (KGD) issues
- Package-on-package stacking provides flexibility in mixing and matching IC technologies
- Devices can be procured from multiple mfg sources: top PoP can be smaller than conventional center BGA (up to 65% smaller than standard PoPt)
- Smaller Package Size: Bottom Fan-in PoP (FiPoPb) allows for smaller package size than standard PoPb (up to 25% smaller) and easier device integration
- Lower Height: FiPoP stacked height same or less than standard PoP
- Lower Warpage: FiPoP significantly less warpage than standard PoP

Features

- Bottom FiPoP has exposed land pattern on center of top surface to allow for mounting of top PoP
- Bottom FiPoP allows for integration of stacked die or fully tested Internal Stacking Module (ISM) within
- Bottom Fan-in PoP can be in either flip chip or wirebond version
- Bottom FiPoP height of less than 1.2mm (TFBGA-FiPoPb) with two dice stacked within
- Top PoP is thinner, more conventional, center BGA
- Top PoP height of less than 0.65mm or 0.8mm for 2 die stack (U/WFBGA-SD2)
- Top PoP height of less than 0.80mm or 1.0mm for 4 die stack (W/VFBGA-SD4)
- Top PoP height of less than 1.0mm or 1.2mm for 7 die stack (V/TFBGA-SD7)
- Ball Pitch down to 0.40mm
- Total stacked package height dependent on FiPoP configuration, but 1.6mm typical (min.1.4mm possible)
- Ni/Au or CuOSP on bottom pads of bottom PoP; lead-free ball options available
- Ni/Au on top lands of PoPb
- Ni/Au or CuOSP on bottom pad of top PoP; lead-free ball options available
- Low stress and warpage packaging materials
- Capable of higher device integration in bottom FiPoP

Applications

- FiPoPb: Cellular phone and mobile device digital baseband processor, digital die stack, or digital + analog baseband die stack, digital + memory (ISM) stack, etc.
- PoPt: Cellular phone and mobile device memory for digital processor and system memory (SDRAM, NOR/NAND Flash, SRAM)



Description

Fan-in Package-on-Package (FiPoP) is a 3D stackable packaging solution. The bottom FiPoP (FiPoPb) provides the flexibility to package a single device or multiple devices (logic, analog or memory), while providing land pads on the top center of the package to allow for another package or components to be reflowed on top. The FiPoPb can also incorporate a fully tested Internal Stacking Module (ISM) package. In addition, the FiPoPb can be smaller than current standard bottom PoP as interconnect is done by means of wire bonds, not solder balls at the edge of the bottom PoP. The package mounted on top of the FiPoPb can be a more conventional "off the shelf" center ball grid array package, such as a typical stacked die memory package or multiple packages or components. The top package can be significantly smaller than the current standard top PoP since it is no longer coupled to bottom package size by peripheral solder ball connections. The result is a flexible 3D stacked package solution with smaller footprint, less board mount issues (warpage) and lower overall cost.

Advantages

Fan-in PoP is a new Package-on-Package approach which addresses the demands of increased miniaturization, smaller footprint and increased device integration for advanced mobile applications. The versatile design of FiPoP accommodates multiple die and larger die sizes in a reduced footprint as compared to conventional PoP solutions, and the flexibility to stack off-the- shelf memory packages with center ball grid array patterns on the top surface.

FiPoP continues to leverage the preferred PoP business model in which logic device manufacturers provide the bottom package and memory device manufacturers typically provide the top package, allowing the end user to configure as needed tested good packages.

The FiPoPb is an FBGA type package and the mountable surface on top is relatively free of warpage that can cause yield problems. The FiPoP construction allows for smaller bottom and top packages. The bottom and top package size can be reduced significantly (up to 25% and 65% respectively), thus taking up less board space and decreasing the overall cost of this PoP solution.

Specifications

Wirebond Die Thickness	60-100mm range performed (2.5-4.0mils)
Flip Chip Die Thickness	Minimum 75µm
Gold Wire	18/25µm (0.7-1.0 mils) diameter
Solder Bumps	Lead-free or Eutectic SnPb flip chip bumps
Lead Finish	Sn/Ag/Cu (Pb-free) ball
Marking	Laser
Packing Options	JEDEC tray or tape & reel

Thermal Performance θja (°C/W)

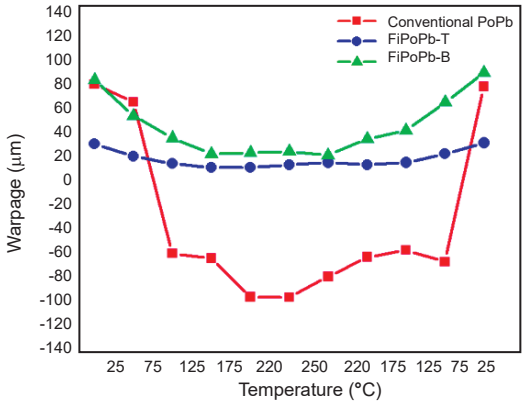
Electrical parasitic data is highly dependent on package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path.

Electrical Performance

Thermal performance of FiPoP configurations are highly dependent on the location of power dissipation, especially for the upper package devices. Detailed thermal modeling is used to accurately determine the actual thermal behavior of each specific FiPoP project.

Reliability

Moisture Sensitivity Level	JEDEC Level 2A (260°C IR)
Temperature Cycling	–65°C/+150°C, 1000 cycles
Temperature/Humidity Test	85°C/85%, RH, 1000 hrs
Highly Accelerated Stress Test	135°C/85%, RH, 96 hrs
High Temperature Storage	150°C, 1000 cycles



FiPoP offers better warpage performance than PoP

Package Configurations

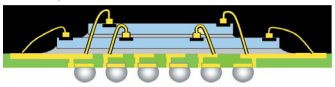
Package	Body Size (mm)	Lead Count
V/TFBGA-FiPoPb-SDx/SDx+y	8 x 8 to 15 x 15	200 ~ 700
U/W/V/TFBGA-SDx (PoPt)	5 x 5 to 14 x 14	

Test Services

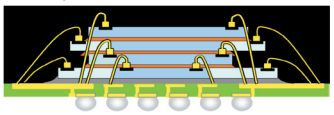
- Product Engineering support
- Probe capability
- Program generation/conversion

Cross Sections

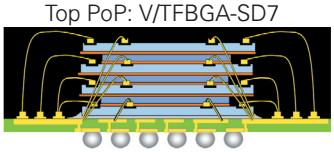
Top PoP: U/WFBGA-SD2



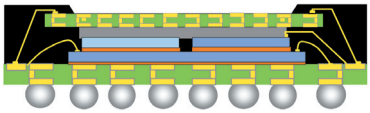
Top PoP: W/VFBGA-SD4



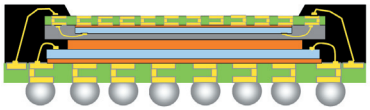
Top PoP: V/TFBGA-SD7



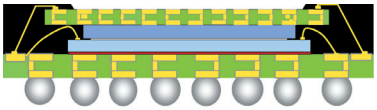
Bottom FiPoP: TFBGA-FiPoPb-SD2



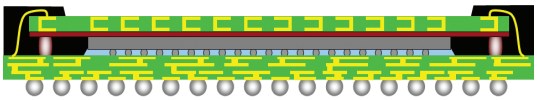
Bottom PoP: TFBGA-FiPoPb-SD1+1
(1 die in ISM)



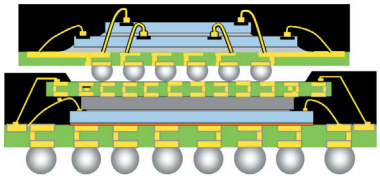
Bottom FiPoP: VFBGA-FiPoPb

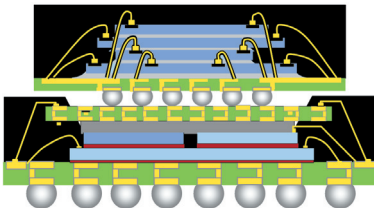


fcVFBGA-FiPoPb



Assembled FiPoP Package Solutions (with top and bottom package)





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