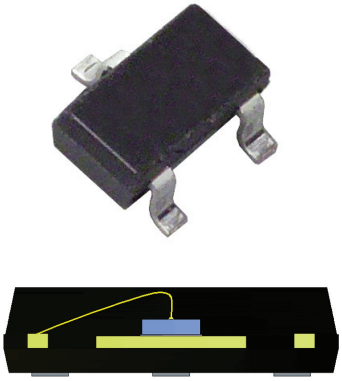
SOT

Small Outline Transistor

Small Outline Transistors (SOT) are industry proven surface mount leadframe packages for small footprint applications. They are available in many body sizes and with package thicknesses ranging from 0.5 to 1.8mm. SOTs are a cost effective solution for a wide range of applications.



Highlights

- Offered in most standard JEDEC outlines
- Pass Moisture Sensitivity Level 3
- Cu wire available for low cost option

Features

- SOT body size production at min. 1.2*0.8*0.5mm , and max. at 6.5*3.5*1.8mm
- Package thickness available of 0.5/0.6/0.75/0.96/1.0/1.1/1.15/1.5/1.66/1.8mm
- Si/GaAs/RDL wafer assembly capability

Standard Materials

- Leadframe: PPF / Ag plating / Selective Ag plating
- Wire: Au wire / Cu wire / AuPdCu wire
- Epoxy: DAF / Screen print / Conductive/ Non-conductive epoxy / Sintering epoxy / Solder paster
- Lead Finish: Sn Plating / PPF

Applications

- ESD Protection
- Digital Camera
- Charger
- Schottky diode in backlight
- Zener diode in mobile application

Process Highlights

Package Thickness	Minimum of 75um
Die Thickness	Minimum of 60um
Wire	Cu / Au / Al wire/ribbon options
Die Attach Tollerance	+/- 38um
Wire Diameter	18 - 50um

Package Level Reliability

Moisture Sensitivity Level	Level 3, 30C / 60%RH, 192hrs
Temperature Cycling	–65C to 150C, 1000 cycles
Autoclave	121C / 100%RH / 2atm, 168 hrs
High Temperature Storage	150C, 1000 hrs
HAST	85C / 85%RH, 1000 hrs

JCET Group Co., Ltd.
www.jcetglobal.com