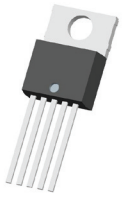
TO

Transistor Outline

Transistor Outline (TO) packages are capable of supporting high pwer devices including diodes, thyristors, power mosfet, insulated gate bipolar transistors and other power devices. They are available in many body sizes ranging from 3.0 x 3.0 to 18.04 x 7.52. Pin counts range from 2 to 6.

TO251



TO220

Highlights

- High current/voltage capacity (200A/2000V)
- Low switching loss
- High thermal conductivity
- Lead-free application
- SiC / GaN wafers

Features

- High power and electrical dissipation
- Package body sizes range from 3.0 x 3.0 to 18.04 x 7.52
- Pin counts from 2 to 6
- Heatsink compatible

Standard Materials

- Leadframe: Cu / Ag plating / Selective Ag plating / Selective Ni plating
- Wire: Cu / Au / Al / Al ribbon
- Epoxy: Conductive / Lead Tin Alloy Silver / Solder Paste
- Compound: Green / Non-green molding compound
- Lead Finish: Sn plating

Applications

- Computing
- Industrial
- Consumer electrical
- Networking devices

Process Highlights

Package Thickness	0.95 - 5mm
Die Thickness	Minimum of 70um
Wire	Cu / Au / Al wire/ribbon options
Lead layer	Single Layer / Dual Layer

Package Level Reliability

Moisture Sensitivity Level	MSL 1/2/3 @ 260C
Temperature Cycling	–65C to 150C, Dwell= 15 min, 500 cycles
PCT	121C/100%RH/205 Kpa, 168 hrs
THT	85C, 85%RH, 1008hrs
HTST	Ta=150C, 1008hrs

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