“Encapsulated Wafer Level Chip Scale Package (eWLCSP™) for Cost Effective and Robust Solutions in FlexLine™”

by

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ABSTRACT

The demand for Wafer Level Chip Scale Packages (WLCSP) has experienced tremendous growth due to the surge in demand for advanced mobile products and pressure of cost reduction. The increased demand is seen for both 200mm wafers and 300mm wafers, however a significant segment of the market continues to be driven by 200mm designs. The infrastructure capacity supporting 200mm WLCSP has been stressed as a result of the mature status of 200mm technology and the rate of conversion of alternative package formats to WLCSP. This creates a dilemma for WLP service providers because adding 200mm capacity continues to require a significant amount of capital. Since 200mm volumes will most likely decline within the next 5 years, it is difficult to justify the use of capital when the depreciation term is longer than the anticipated life cycle of the product. Typically, Si WLCSP package is conducted with full function test at wafer level sorting and followed by mechanical blade dicing with or without laser grooving. Mechanical blade dicing may cause front side chipping and backside chipping, which in turn will cause package failures that are not detected before the SMT process. The surge in demand on WLCSP makes the industry realize the potential failures, and the need to actively look for a solution. While conventional backside processes can address backside chipping, it can't provide protection from the sidewall cracking. This is motivating the industry to look into 5-side inspection in the tape and reel (TnR) process, although this obviuously increases the package cost while not necessarily screening out the failure units due to no functional test being applied.

This paper introduces a new encapsulated WLCSP product (eWLCSP™) and innovative manufacturing process known as the FlexLine™. The new eWLCSP product has a thin protective coating applied to at least 4 sides of the silicon sidewall with the optional to encapsulate all exposed silicon surfaces on the die. The applied coating protects the silicon and fragile dielectrics and prevents handling damage during dicing and assembly operations, effectively providing a durable packaged part in the form factor of a WLCSP. The FlexLine manufacturing process used to produce eWLCSP leverages existing high volume manufacturing methods with exceptionally high process yields. In this process the silicon wafer is diced prior to the wafer level packaging process. The dice are then reconstituted into a new wafer form with adequate distance between the die to allow for a thin layer of protective coating to remain after final singulation. Standard methods are used to apply dielectrics, thin film metals, and solder bumps. The resulting structure is identical to a conventional WLCSP product with the addition of the protective sidewall coating. The most important step of the process is when the diced Si die go through a kind of "burn-in" test after running through the whole FlexLine assembly process before final wafer level test. In package singulation, there is no additional mechanical or thermal damage on either front side or sidewall/backside of Si die due to the protection of the encapsulant. The singulated package becomes the real known good die without the need to conduct a manual 5-sided inspection. This paper discusses the key attributes of the new eWLCSP as well as the manufacturing process used to create it. Reliability data will be presented and compared to conventional WLCSP products and improvements in package reliability and performance will be discussed and compared to conventional WLCSP.

Improving the Conventional WLCSP Structure

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging [1]. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides and back of the die. The WLCSP is the smallest possible package size since the final package is no larger than the required circuit area. Although WLCSP is now a widely accepted package option, the initial acceptance was limited due to concerns with the Surface Mount Technology (SMT) assembly process and the fragile nature of the exposed silicon inherent in the package design. Assembly skills and methods have improved since the introduction of WLCSP, however, damage to the exposed silicon remains a concern. This is particularly true for advanced node products with fragile dielectric layers.

A new process has been developed to provide five-sided protection for the exposed silicon in a WLCSP, therefore achieving a true known-good WLCSP. The ability to apply a protective coating to all the exposed die surfaces in a WLCSP with encapsulation, RDL, and bumping "burn-in" process is based on an existing high volume manufacturing flow developed for fan-out products known as embedded Wafer Level Ball Grid Array (eWLB),. Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Although this is commonly done for other semiconductor package formats, it has not been practiced for conventional WLP. Following singulation, the diced silicon wafers are then reconstituted into a standardized wafer (or panel) shape for the subsequent process steps as shown in Figure 1.

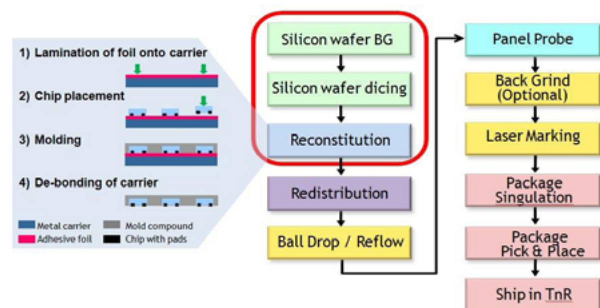

Figure 1. eWLB Process Flow

The reconstitution process as shown on the left in Figure 1 includes four main steps.

1) The reconstitution process starts by laminating an adhesive foil onto a carrier.

2) The singulated die are accurately placed face down onto the carrier with a pick and place tool.

3) A compression molding process is used to encapsulate the die with molding compound while the active face of the die is protected.

4) After curing the molding compound, the carrier and foil are removed with a de-bonding process, resulting in a reconstituted wafer where the molding compound surrounds all exposed silicon die surfaces.

The eWLB process is unique in that the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations [2].

FlexLine™ : Breakthrough Manufacturing Method for Wafer Level Packaging

A new manufacturing method, FlexLine™, has been developed to produce a wafer level package that severs the link between wafer diameter and wafer level packaging methods. The new manufacturing method is wafer size agnostic, so one manufacturing module can produce fan-in, fan-out, and 3D fan-out products regardless of the incoming wafer size. The same bill of materials, manufacturing methods and manufacturing location can produce wafer level packages from any size silicon wafer. Since the manufacturing module is wafer size agnostic, there is no risk of capital for investment in the manufacturing infrastructure. A change in loading between 200mm, 300mm, and 450mm wafers does not adversely affect the utilization of the manufacturing module. The process also enables new advanced wafer level packages otherwise unattainable with conventional manufacturing methods. FlexLine™ seamlessly processes multiple silicon wafer diameters on the same manufacturing line and produces both fan-out and fan-in devices as illustrated in Figure 2. FlexLine™ provides the ability to scale a device to larger panel sizes for a compelling cost reduction compared to conventional wafer level packaging methods. The FlexLine™ process has been qualified at advanced silicon nodes down to 22nm, ball pitches down to 0.40mm and body sizes as small as 2.5x2.5mm.

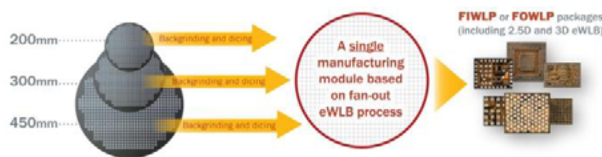

Figure 2: FlexLine™ seamlessly processes multiple silicon wafer diameters on the same manufacturing line to produce both FIWLP and FOWLP.

Innovative WLCSP with sidewall protection

Using the FlexLine™ process, a protective coating can be cost effectively applied to the exposed Si surfaces in a WLCSP, thereby addressing the chipping, cracking and other handling damage that can occur during the assembly process. The WLCSP follow the same process flow as described in Figure 1. Reconstituted wafers are processed with conventional wafer level packaging techniques for the application and patterning of dielectric layers, thin film metals for redistribution and under bump metal and solder bumps. In the final dicing operation a thin layer of molding compound, typically 30um, is left on the side of the die as a protective layer. The back of the die is also protected with molding compound, although with a greater thickness. The result is a new encapsulated Wafer Level Chip Scale Package (eWLCSP™) which has an increased level of durability and reliability over traditional WLCSP designs. The significant benefit of encapsulation is the light and mechanical protection for the bare die. The eWLCSP™ structure is equivalent to conventional WLCSP with the addition of a thin protective coating on the four sidewalls of the die. [3] A schematic drawing of a typical structure is shown in Figure 3 for greater clarity. Alternatively, the backside molding compound can be removed and the body made thinner with an optional back grind operation without damaging the protective sidewall layer. The remaining sidewall coating will continue to protect the fragile silicon sides of the die during the assembly operation. Figure 4 shows the micrographs of eWLCSP with SEM and optical view.

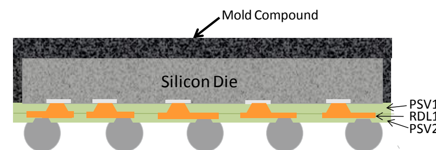

Figure 3. eWLCSP™ Structure

Innovative WLCSP with natural "burn-in" test

Another unique attribution of the FlexLine process is the Si die are diced with a mechanical blade before the reconstitution process and actually go through a kind of "burn-in" test after running through the reconstitution, RDL build-up and solder bumping process before final wafer level test. In final panel dicing, there is no additional mechanical or thermal damage on either front side or sidewall/backside of Si die due to the protection of remained encapsulant. The dicing blade does not touch the Si material anymore in panel dicing. The singulated package becomes the real known good die without the need to conduct reluctant and often ineffective 5-side inspection.

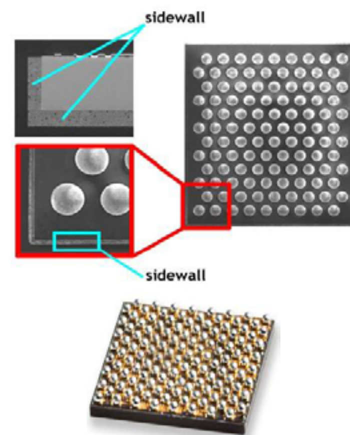

Figure 4. Micrographs of eWLCSP™

The Encapsulated WLCSP Structure

In FOWLP, the area of the package is increased to allow for placement of redistribution layers (RDL) and solder balls outside of

the silicon die area. This allows the die to shrink to a minimum size independent of the required area for an array of solder balls at industry standard BGA ball pitches [4]. It also enables novel multi-die structures, 2.5D structures and 3D structures. In the case of conventional FOWLP, die are typically widely spaced to allow for the expanded RDL and bump area and the conventional saw street. In the case of eWLCSP™, the die are closely spaced, allowing for only the sidewall thickness in addition to a saw street area. The eWLCSP™ process data presented here was generated with a 300mm round reconstituted panel [5]. The die size was 4.5x4.5mm. The final structure had 2 layers of polymer and 1 layer of plated Cu RDL with the solder ball mounted directly on the RDL without the use of a separate UBM layer.

Advantages of the Encapsulated WLCSP, eWLCSP™[5]

Intuitively, eWLCSP™ would seem to have a higher cost over conventional WLCSP since there are additional steps required for reconstitution at the start of the FlexLine™ manufacturing flow. There are two key factors, however, that offset the cost of the additional steps required for the reconstitution to make this a commercially viable process.

(1) Cost-effectiveness
As described above, eWLCSP™ is fabricated using reconstitution. Good die from the parent wafer are picked and transferred to a (larger) reconstituted carrier. Since the majority of WLCSP products use 200 mm wafers, reconstitution enables the scaling of the manufacturing process from the 200 mm wafer to the size of the carrier utilized in eWLB technology. This carrier size ranges from 200/300 mm to a larger format like high density (HD) with ~ 20% greater area or Ultra High Density (UHD) with > 300% greater area. The HD format is currently in mass production. The scaling of the manufacturing process with reconstitution far outweighs the cost of reconstitution itself, thereby enabling large net cost reductions. Additionally, the ability to selectively pick good die from the parent wafer presents an additional net cost benefit as most wafers have a less than 100% wafer sort yield. Last but not least, the ability to pool the manufacturing volume of traditional fan-out eWLB packages seamlessly together with eWLCSP™ packages on the same FlexLine™ provides important economies of scale. With the three factors stated above, net cost reductions up to 40% over traditional WLCSP front end processing are achievable depending on the original wafer diameter, the carrier format used for reconstitution (300mm, HD or UHD) and the yield of incoming wafers.

(2) High Quality Solutions
The polymer sidewall structure of eWLCSP™ all but eliminates mechanical damage such as chipping and cracking that is commonly encountered in traditional WLCSP processing. This serves to eliminate many expensive steps such as back side coating or lamination and complex inspection steps that are currently necessary for standard WLCSP to manage mechanical damage and ensure product quality. More fundamentally, the eWLCSP™ allows customers to ***build in quality by design*** vs. using inspection to weed out defects. This has implications for reducing the risk of field failure due to the shipment of marginally defective parts that may escape inspection. As is shown in a later section, the encapsulated eWLCSP™ structure has also helped to increase the overall die strength by ~ 100% in addition to the mitigation of cracking and chipping defects, making for an overall more robust package.

(3) Investment and Infrastructure – Wafer Agnostic Processing
In traditional WLCSP processing, the investment and infrastructure for manufacturing are based on the diameter of the incoming wafer. This creates a financial burden to re-tool the manufacturing lines to provide the needed capacity (to meet market demand) as wafer transitions occur (e.g. from 200 mm to 300 mm or from 300 mm to 450 mm in future) while also having to obsolete the existing manufacturing assets. The FlexLine™ approach for eWLB and eWLCSP™ effectively decouples the packaging process from the incoming wafer altogether obviating the above-described financial burden resulting from wafer diameter transitions.

(4) Design Friendly – Allows seamless transition from fan-in to fan-out within the same basic package platform
As noted previously, the standard fan-in WLCSP only works below a certain threshold of I/O density, based on the minimum allowable terminal I/O pitch. - The threshold is ~ 4 I/O /mm2 for a 0.5 mm terminal I/O pitch and ~ 6 I/O /mm2 for 0.4 mm terminal I/O pitch. Small changes in I/O density that commonly occur with changes in Si design, die shrinks resulting from Si node transitions may lead to a given design exceeding the WLCSP threshold, causing the design to “fall off” the WLCSP application space envelope, necessitating a change in packaging POR to traditional substrate- or leadframe-based packages like FBGA, fcBGA, QFN etc. These packages are fundamentally different than WLCSP in terms of footprint, form factor, performance and cost, resulting in a major “reset” in the packaging plan of record (POR). In contrast, the eWLCSP™ may be viewed as part of the more universal eWLB platform wherein the aforementioned I/O density transitions can be seamlessly accommodated within the same packaging platform. For designs whose I/O density falls marginally outside the threshold, an additional row of terminal solder balls can be added without fundamentally altering the package structure, form factor or performance.

eWLCSP™ Product Assessment

The protective sidewall coating is a unique attribute of the eWLCSP™ package. This protective layer is durable and will prevent silicon chipping on the side of the package and has the ability to protect the silicon during socket insertion for test. This has been demonstrated through multiple insertion tests on completed products with no observed damage to the protective coating. The eWLCSP™ process has passed standard reliability tests used in wafer level packaging including Component Level Reliability (CLR), Temperature Cycle on Board (TCoB), and Drop Test. Component Level Reliability was completed with the test conditions shown in Table 2.

Table 2. Component Level Reliability Results

Component Level Test	Condition		Status
MSL1	MSL1, 260C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55°C to 125°C	1000 x	Pass
HAST (w/o bias) after Precon	130°C / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150°C	1000 hrs	Pass

The evaluation results were confirmed by visual inspection and electrical test. No delamination of the protective coating was detected during the CLR evaluation. TCoB was completed and passed 500 cycles with the results shown in Table 3. Results obtained from electrical measurement of daisy chain bump structures demonstrate eWLCSP is comparable to conventional WLCSP product produced

with polyimide dielectrics. Drop test was completed and passed the JEDEC requirement of 30 drops with the results shown in Table 3.

Table 3. Board Level Reliability Test Results

Tests	Conditions	Failure Rate	Characteristic life (η)	Weibull slope (β)	First Failure
TCoB	-40ºC to 125ºC	0.635	1219.4	10.13	864x
Drop Test	JEDEC	0.635	1553.5	5.97	772x

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eWLCSP™ Mechanical Robustness

Thin profile packages are more attractive for mobile/portable electronics as well as integrated module assembly. A Si exposed package is well accepted in WLCPS as well as flip chip packages. For eWLCSP, Si and molding compound are to be removed simultaneously due to its embedded structure. In this study we evaluated thin eWLCSP (as shown Figure 5.(b)) mechanical strength compared to standard WLCSP with back side coating (BSC). First, a 4-point bending test was carried out and the results are plotted as shown in Figure 6. eWLCSP™ with sidewall protection shows over 25% increase in die strength compared to standard WLCSP. eWLCSP has a significant die strength increase with sidewall protection and optimized backgrinding process. The Si surface roughness was measured with AFM and the data is presented in Table 3. It shows eWLCSP™ has quite close roughness value as WLCSP. Theroughness scan image of Figure 7 clearly showed no difference in Si surface roughness between WLCSP and eWLCSP. With these test results along with component and board level reliability results in previous sections, eWLCSP™ has more robust reliability than standard WLCSP with additional sidewall protection to prevent any side chip cracking.

(a) (b)

Figure 5. SEM micrographs of cross-section of: (a) eWLCSP™ and (b) thin eWLCSP™.

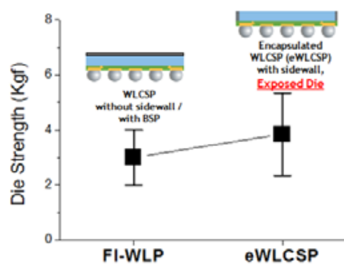

Figure 6. Die strength test with 4-point bending

(a) **(b)**

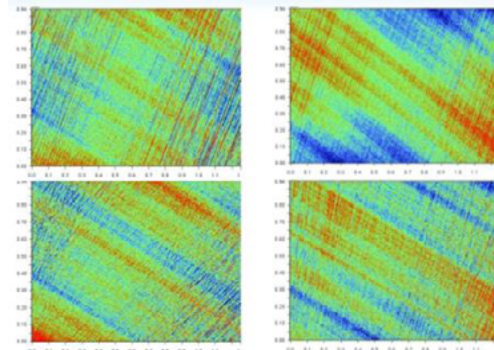

Figure 7. Surface roughness measurement results of (a) WLCSP and (b) eWLCSP™ with exposed Si.

Conclusions

Growing demand for WLCSP in a range of advanced mobile products is driving the need to cost effectively reduce risk of cracking, chipping and handling issues before or during the SMT assembly process. This is particularly true for advanced node products where the die is very thin and dielectric layers are extremely fragile. A new encapsulated WLCSP has been developed and manufactured using a proven manufacturing method known as FlexLine™. The mechanical sidewall protection that is now possible in eWLCSP™ devices resolves the problem of silicon damage during the assembly process and provides a path to significant cost savings for customers as the manufacturing panel size is increased. The same manufacturing line can process eWLCSP™ products regardless of the incoming wafers size and 450mm wafers can easily be accommodated for the encapsulated WLCSP process once the service is required by the customers.

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