“Flexline - A Flexible Manufacturing Method for Wafer Level Packages”

(Extended Abstract)

by

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Trends in Wafer Level Packaging

There are some common and well known trends in Wafer Level Packaging driven by the surge in advanced mobile products. Silicon nodes are shrinking from 32nm to 28nm to 20nm and below and packaging materials and processes need to adapt to these node without causing damage to the new more fragile structures. Product form factors are shrinking with the requirement for higher I/O count and greater complexity in ever smaller package sizes. There is increase integration of active and passive components into single packages in novel PoP and SiP configurations. At the same time there is extreme pressure to reduce cost. Effective cost reduction strategies are critical for current and future technologies. Typical annual cost reductions of ~5% are expected for a mature technology based on manufacturing efficiency, scaling, and materials cost reduction, but it is difficult to achieve additional and dramatic cost reductions on a mature WLP technology.

The demand for Wafer Level Chip Scale Packages (WLCSP) has experienced tremendous growth due to the surge in demand for advanced mobile products. The increased demand is seen for both 200mm wafers and 300mm wafers, however it is less intuitive that a significant segment of the market continues to be driven by 200mm designs running at 90nm and above. Established, depreciated, 200mm silicon foundries provide an optimum design node for many analog and power management products at exceptionally low cost and the demand for 200mm silicon is forecast to increase through at least 2015.

Given the mature status of the 200mm technology and the conversion rate of package designs to WLCSP from other package formats, the infrastructure supporting 200mm WLP capacity has been stressed to the breaking point. Customers are commonly dealing with a shortage in 200mm WLCSP capacity as a result of the growth rate. This creates a dilemma for WLP service providers because adding 200mm capacity still requires a significant amount of capital with the risk that demand will begin to decline prior to the full depreciation of the new assets.

The Wafer Level Packaging Paradigm

Silicon wafer diameter is based on the diameter of the single crystal silicon ingot pulled at the start of the IC manufacturing process. The ingot shape produces a round wafer that is processed through specialized equipment during wafer fabrication. Classic methods of wafer level packaging leverage this semiconductor equipment infrastructure to process the wafers in their original form and are subsequently locked into a single silicon wafer diameter. This classic method has been beneficial since it leverages equipment and processes developed for the IC industry, however the equipment is very expensive for larger wafer diameters and the fine geometries required in advanced node IC products are not required for wafer level packaging.

Process requirements for WLP redistribution layers and under bump metal do not require the full fine patterning capability of advanced node semiconductor processes, so the semiconductor equipment capability is typically over kill for the WLP process. The problem is serious for 200mm and 300mm wafer bump lines, however the capital equipment cost for a future 450mm bumping line may well be prohibitive for wafer level packaging. The inflexibility of manufacturing lines locked to a specific silicon diameter creates a situation where WLP service providers are constantly faced with decisions on the best allocation of capital between the various silicon wafer sizes required by their customers. The paradigm that the die should remain in the original round silicon format must be questioned.

A Flexible Wafer Level Packaging Module

There is no need to maintain a round silicon format in processing WLCSP. A new manufacturing method has been developed to produce a WLCSP that severs the link between wafer diameter and wafer level packaging methods. The new manufacturing method is wafer size agnostic, so a single manufacturing module can produce a consistent Wafer Level Package regardless of the incoming wafer size. The new manufacturing module can seamlessly process any silicon diameter without a change in the equipment set or bill of materials used in the packaging process. WLP products produced in the module can include fan-in, fan-out, as well as 2.5D and 3D fan-out products.

Once recombined into a panel format, the product can be processed with conventional wafer level packing techniques, including dielectric deposition, metal plating and solder ball drop. Since the manufacturing module is wafer size agnostic, there is no risk of capital for investment in the manufacturing infrastructure. A change in loading between 200mm, 300mm, and 450mm wafers does not adversely affect the utilization of the manufacturing module. As the panel size is increased and the modules are scaled, the cost of producing wafer level packages drops significantly when compared to the cost of making equivalent packages using conventional silicon fan-in WLP methods. The process also enables new advanced Wafer Level Packages otherwise unattainable with conventional manufacturing methods.

Unlike conventional Wafer Level Packaging, the first step in the new process is to thin and singulate the incoming silicon wafer. Although this is commonly done for many semiconductor package formats it has not been practiced for Wafer Level Packaging. The back grind and dicing steps are the only steps in the process where wafer size specific equipment is required. Once the individual die is created, a reconstitution process is started. The die is placed face down onto an adhesive film, a compression molding process is used to lock the die into relative position, and a new standard panel format is created that is independent of the original silicon wafer size. Placement accuracy is critical on both a micro and a macro level since photolithography is subsequently required to pattern the redistribution layers and align to the die pad openings. A simple process flow is shown in Table 1 with the pre-process steps highlighted.

1	Incoming Si	Pre-Process	14	Resist Strip
2	Backgrind		15	Seed Layer Etch
3	Dicing		16	Polymer 2 Deposition
4	Lamination		17	Polymer 2 Litho
5	Die Pick and Place		18	Polymer 2 Cure
6	Compression mold		19	Ball Drop and Reflow
7	Debond		20	Final Inspection
8	Polymer 1 Deposition		21	Backgrind
9	Polymer 1 Litho		22	Laser Mark
10	Polymer 1 Cure		23	Package Singulation
11	Seed Layer Deposition		24	Package Pick and Place
12	Plating Litho		25	Ship
13	Cu RDL Plate			

Table 1

The process cost for an individual panel is higher than a conventional silicon process since the pre-process steps are not required in the conventional process flow, however the cost of the added steps is offset by panel size scaling and a significant cost reduction is possible on a unit basis as the panel size increases. In the first implementation of this technology, a 200mm wafer was converted into a round 300mm reconstituted panel. In this example the cost of producing an equivalent WLCSP was reduced by 15%. The current 300mm process would work equally well to provide significant savings for 150mm wafers, since the panel size scaling is even more dramatic. An example of cost savings with panel size conversion of 200mm silicon to 300mm reconstituted panel (4x4mm die size) is shown in Figure 1.

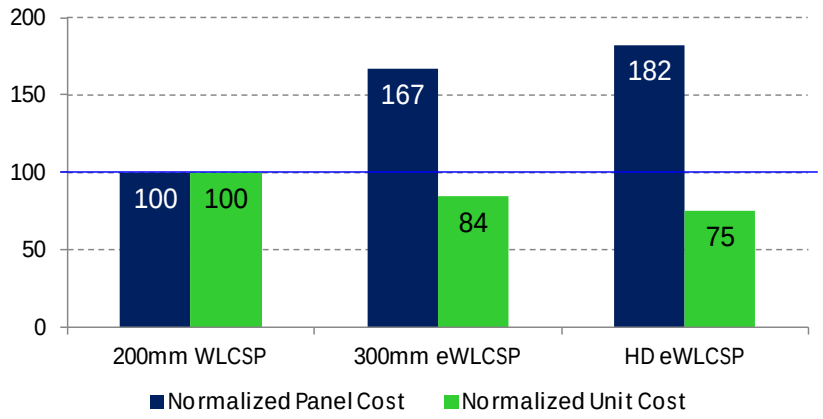

Figure 1

The range of products produced by the manufacturing module is shown in Figure 2 below.

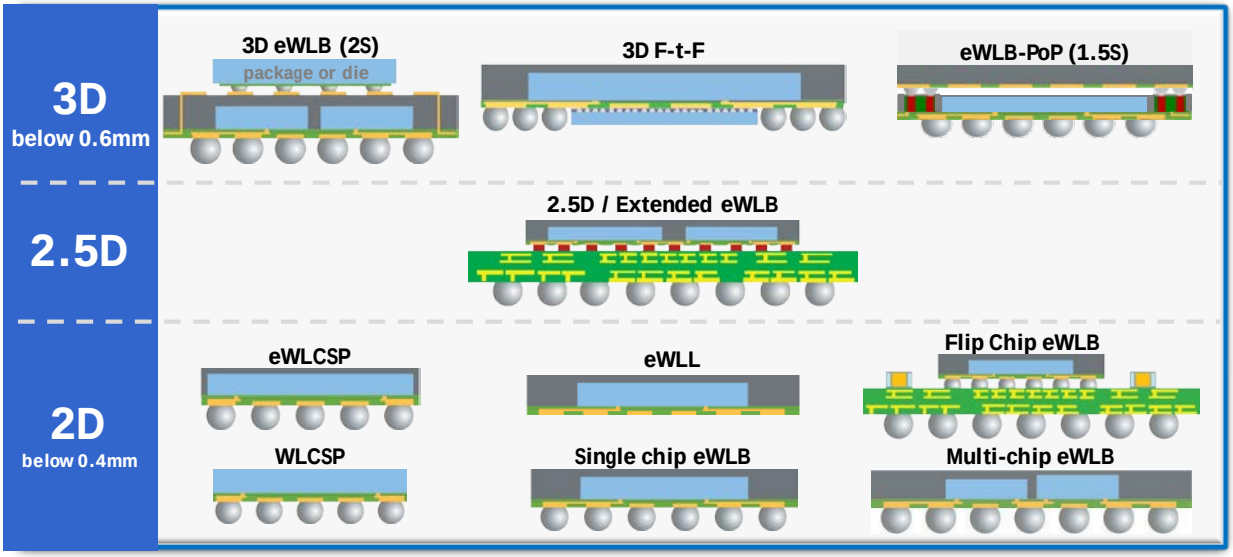

Figure 2

A wide range of eWLB fan-out products can be produced in the module including both PoP and non-PoP structures. A novel version of a WLCSP is shown in Figure 2 in the eWLCSP product. In this product, the bare silicon edges and back typically provided in a conventional WLCSP product are protected by mold compound. The protective layer can be very thin so there is only a minimal increase in package dimensions. The encapsulated WLCSP package is easily and cost effectively produced in the manufacturing module, yet it is impossible to produce using conventional WLCSP processes.

Conclusion

A new manufacturing method has been developed for Wafer Level Products that severs the link between the bumping process and the silicon wafer size. This method produces a wide range of products with very competitive pricing since singulated die are placed into a standardized panel format. Capacity can be increased by building duplicate manufacturing modules with very low risk to the capital investment since the mix of incoming silicon diameter is no longer an issue.