## "Solder Joint Fatigue Life Prediction in Large Size and Low Cost Wafer-Level Chip Scale Packages"

by

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# Solder Joint Fatigue Life Prediction in Large Size and Low Cost Wafer-Level Chip Scale Packages

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Abstract-With the highly insatiable demands of higher performance and lower cost requirements for handheld and portable electronic devices in the semiconductor industry, the wafer level chip scale package (WLCSP) is widely used in integrated circuit (IC) fabrication today with rapidly growing demands. Recently, WLCSP without utilization of an underbump metallization (UBM) layer has been proposed for cost reduction purposes, eliminating the process of electroplating the UBM layer as compared to conventional WLCSP processes. For applications with larger than 5x5 mm<sup>2</sup> die sizes, the die I/O can be increased to enhance the corresponding performance. With the increasing requirements of multifunctional, smaller form factor, lower cost and fine pitch package designs in WLCSPs, a number of challenges need to be overcome, especially in terms of preventing possible failures and enhancing reliability. It is well known that the empirical Coffin-Manson equation has been widely adopted to evaluate the thermal fatigue life of the solder joint in electronic packages. For the sake of understanding the thermal fatigue life of a large size and low cost WLCSP with Sn1.0Ag0.5Cu (SAC105) solder joints, the board level reliability (BLR) thermal cycling test (TCT) that follows JEDEC standards was evaluated. The solder joint characteristic life in a large size and low cost WLCSP can be obtained by Weibull analysis according to the experimental result. The three-dimensional (3D) finite element analysis (FEA) with rate dependent nonlinearity material properties was utilized to study the solder joint creep behaviors. With the correlation of experimental and simulation results, the modified Coffin-Manson equation for SAC105 solder joint fatigue life estimation in a large size and low cost WLCSP can be established. Based on the present equations, the thermal fatigue life for the utilization of SAC105 solder joints in a large size and low cost WLCSP can be effectively estimated through the numerical modeling without any experimental evaluation. This study will be useful if high reliability and cost reduction in a large size and low cost WLCSP is required.

Keywords—Wafer level chip scale packages, solder joint fatigue life, finite element analysis, Coffin-Manson equation, thermal cycling test, board level reliability

#### I. INTRODUCTION

In pursuing the higher performance, better reliability and lower cost demands for handheld and portable electronic devices, the wafer level chip scale package (WLCSP) has become a preferred solution that is widely used in the semiconductor industry. These insatiable demands have been Su-Lan Tzeng Wafer Level Package R&D STATS ChipPAC Taiwan Co., Ltd Hsinchu, Taiwan sl.tzeng@statschipac.com

pushing WLCSP designs aggressively towards larger die sizes and lower prices [1-3]. To enhance WLCSP performance, applications with larger than 5x5mm<sup>2</sup> die size and increased die I/Os are typically utilized. To support low cost requirements, a WLCSP that eliminates the process of electroplating the underbump-metallurgy (UBM) layer as compared to conventional WLCSP (with one UBM layer, one redistribution layer (RDL) and two polymer layers on the passivated wafer) was introduced in recent years. The process flow and corresponding solder joint cross-sectional images for this low cost WLCSP are illustrated in Fig. 1 [4]. To satisfy the demands for smaller form factor, multifunctional and low cost devices, a number of challenges need to be overcome, particularly in terms of preventing possible failures and enhancing package reliability [5, 6].

Since the solder joint fatigue failure is the most common failure mode in WLCSPs and package reliability becomes worse if the design of a larger die WLCSP is employed, it is important to understand fatigue behavior. For estimating the solder joint fatigue life in electronic packages, the empirical Coffin-Manson equation is well known [7, 8]. For the sake of understanding the solder joint reliability fatigue life in a large size (5.3x5.3mm<sup>2</sup>) and low cost WLCSP (without utilization of a UBM layer), the board level reliability (BLR) thermal cycling test (TCT) that follows JEDEC standards for the temperature change from -40°C to 125°C was evaluated. The Sn1.0Ag0.5Cu (SAC105) solder joints are used as the interconnections between the die and printed circuit board (PCB). According to the BLR TCT results, the experimental solder joint fatigue life of this WLCSP can be obtained by a probability plot of Weibull distribution. In order to establish a modified Coffin-Manson equation for solder joint fatigue life prediction, the three-dimensional (3D) finite element analysis (FEA) with rate dependent material nonlinearity behaviors was utilized. Through the correlation of experimental and simulation results, the fatigue ductility coefficient and the reciprocal of the fatigue ductility exponent in the modified Coffin-Manson equation for SAC105 solder joints in a large size and low cost WLCSP can be obtained. By using the present equations, the correlated thermal fatigue life for utilization of SAC105 solder joints in the WLCSP without a UBM layer can be effectively estimated through the numerical modeling instead of evaluating the BLR TCT experiments. This study will be useful if high reliability, cost reduction and

fast development time in a larger die size and low cost WLCSP are required.



Fig. 1. (a) The process flow; (b) the cross-sectional images of solder ball structures in a large size and low cost WLCSP [4].

#### II. **RELIABILITY EVALUATION**

The BLR TCT that follows JEDEC standard-JESD22-A104D condition G for the temperature change from -40°C to 125°C was completed to evaluate the thermal fatigue life in the packages [9]. Three WLCSPs that did not have a UBM layer were introduced as test vehicles. The WLCSPs had a large die size of 5.3x5.3mm<sup>2</sup> and solder ball pitch of 400µm. The SAC105 solder joints were utilized to connect the die and PCB. The detailed dimensions of the WLCSPs and their corresponding cross-sectional images are shown in Table I and Fig. 2, respectively. The PCB uses a built-up multilayer technology that incorporates microvias in a 1+6+1 stack-up structure (following the JEDEC standard No.22-B111) [10]. The PCB thickness was 1.0mm with 132x77mm<sup>2</sup> dimensions that accommodated 15 components of the same type in a 3 row by 5 column format (shown in Fig. 3). The PCB pad design for perimeter I/O devices followed IPC-SM-782 guidelines and all component attachment pads were non-solder mask-defined (NSMD). The NSMD interconnects with solder

resist opening (SRO) of 300µm and thickness of 30µm were utilized on the top surface of the PCB in the WLCSPs. The diameter of the Cu pad on PCB was 220µm and thickness was 25µm. The PCB pad layout and the corresponding crosssection image are shown in Fig. 4. The designs of test vehicles #1, 2 and 3 (TV1, TV2 and TV3) are solder-mask-defined (SMD) on die side (which means that the PBO2 opening size is smaller than RDL pad size) while the design of 2P1M-TV3 is NSMD on die side (which means that the PBO2 opening size is larger than the RDL pad size).

Table I. The dimensions of a lager size and low cost WLCSP (without a UBM layer)

Dimensions	Test Vehicles			
Dimensions	TV1	TV2	TV3	
Die size (mm <sup>2</sup> )	5.3 x 5.3			
PBO1 thickness (µm)		7.5		
PBO2 thickness (µm)		10		
PBO2 opening (µm)	240	205	240	
RDL pad size (µm)	260	225	200	
RDL thickness (µm)	8			
Ball pitch (µm)	400			
Ball size (µm)	250			
Ball number	121			





TV3



Fig. 2. Cross-sectional images of SAC105 in a large size and low cost WLCSP.



Fig. 3. PCB layout



Fig. 4. The PCB pad design layout and cross-section images (a) on side A (with microvias); (b) on side B (non-microvias).

Fig. 5 illustrates the Weibull distribution of BLR TCT result in large size and low cost WLCSPs with SAC105 solder joints (under test condition G with soak mode 4 of 15-min dwell time). In Fig. 5, the Weibull parameter  $\eta$  is the characteristic lifetime (63.2% failed) and  $\beta$  is the shape parameter. The result indicated that the first failures for TV1, TV2 and TV3 are 185, 188 and 210 cycles, respectively, and the characteristic lives are 318, 418 and 500 cycles, respectively. The design of NSMD on die side (TV3) will result in better thermal fatigue life than the design of SMD. The smaller RDL pad size (TV2) was better for the thermal fatigue life as compared to the larger RDL pad size (TV1). Fig. 6 illustrates the reliability scanning electron microscope (SEM) results of the WLCSPs. By examining the SEM photos in Fig. 6, it was determined that the solder crack initially occurred near the corner of the RDL pad and solder ball. The solder crack propagated along the top IMC layer underneath the RDL pad as well as along the top surface of PCB Cu pad in the WLCSP.



		1 V I	1 V 2	1 V 3		
	1st failure (cycles)	185	188	210		
	63.2% (cycles)	318	418	500		
F	Fig. 5 Probability plot of Weibull distribution for SAC105 solder joint fatigu					

Fig. 5. Probability plot of Weibull distribution for SAC105 solder joint fatigue life in a large size and low cost WLCSP.



Fig. 6. Failure results of SAC105 solder joint in BLR TCT (a) TV1; (b) TV2.

#### III. MODELING ANALYSIS AND CORRELATION

### A. Finite Element Analysis (FEA)

For the purpose of correlating the solder joint fatigue life through simulation and BLR TCT, the 3D FEA with pure hexahedral element-meshes was constructed. Due to the symmetry feature, only a quarter was employed. Since the maximum creep strain and/or creep strain energy density is typically located on the outermost solder ball and this is always the critical place to drive the solder crack in WLCSP, dense meshes were used in this critical place to have precise solutions. The quarter finite element models and the applied boundary conditions for the WLCSP are shown in Fig. 7 (with PCB size of 20x23mm<sup>2</sup>). The loading condition with five thermal cycles initially from 25°C to 125°C and down to -40°C were set in FEA, which consists of 15-min (soak mode 4) dwell time with temperature extremes of 125°C and -40°C. The employed material properties in the WLCSP are listed in Table II. In Table II, E, v, CTE and Tg are Young's modulus, Poisson's ratio, coefficient of thermal expansion and glass transition temperature, respectively. The creep constitutive equation (Garofalo-Arrhenius creep model) of SAC105 leadfree solder joint was described as [11, 12]

$$d\varepsilon_{cr} / dt = C_1 [\sinh(C_2 \sigma)]^{C_3} e^{-(C_4/T)},$$
(1)

where  $d\varepsilon_{cr}/dt$  is equivalent creep strain rate,  $\sigma$  is the equivalent stress and *T* is the absolute temperature.  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  are material parameters which are defined as [12]:

 $C_1 = 2.31 \times 10^6 (1/\text{sec}), C_2 = 0.026, C_3 = 6.5, C_4 = 6962.7 (K).$ 



Fig. 7. Finite element model and applied boundary conditions of a large size and low cost WLCSP.

Table II. Employed material properties in WLCSP.

Material	E (GPa)	ν	CTE (ppm/ °C)
Die	131	0.28	2.8
Low-k	10	0.16	5
PBO1/PBO2	2.3	0.3	64
PCB Cu pad	110	0.34	17
Solder resist (SR)	3.2	0.4	58/153
			(Tg=105°C)
Solder (SAC105) [13]	37	0.35	20
RDL (Cu)	110	0.34	17
PCB	22	0.28	18.5
Passivation (SiN/USG)	137.5	0.206	1.907
UBM (Cu)	110	0.34	17

Fig. 8 and 9 illustrate the contour of creep strain energy density and equivalent creep strain for SAC105 solder joints in the WLCSPs at the end of the fifth thermal cycle, respectively. The result indicates that the maximum value occurs at the solder top interface of the outermost solder joint in the package. Fig. 10 shows the average element creep strain energy density and equivalent creep strain over the course of five thermal cycles for SAC105 solder joints. The change in creep strain energy density was virtually invariant after the third thermal cycle and can be shown in most packages [14]. Hence, all the results are determined from the fifth thermal cycle. The results of the change in creep strain energy density ( $\Delta W$ ) and the change in equivalent creep strain ( $\Delta \gamma$ ) at fifth thermal cycle for TV1, TV2 and TV3 are listed in Table III.



Fig. 8. Creep strain energy density result for SAC105 solder joint in large size and low cost WLCSPs.



Fig. 9. Equivalent creep strain result for SAC105 solder joint in large size and low cost WLCSPs.



Fig. 10. (a) Creep strain energy density; (b) equivalent creep strain during five thermal cycles for SAC105 solder joints in a large size and low cost WLCSP.

Table III. The simulation result of  $\Delta W$  and  $\Delta \gamma$  for SAC105 solder joints

Creep strain	Test Vehicles (large size and low cost WLCSP)		
energy density	TV1	TV2	TV3
$(\Delta W; MPa)$	7.1978	6.3373	5.9014
Equivalent creep strain $(\Delta \gamma)$	0.240175	0.214640	0.213649

#### B. Coffin-Manson Equation Correlation

For the solder joint fatigue life correlation with simulation and BLR TCT results, there are two modified Coffin-Manson equations being utilized and can be expressed as [15-16]

$$N_f = A_1 (\Delta W)^{-n_1}; \tag{2}$$

$$N_f = A_2 (\Delta \gamma)^{-n_2}; \tag{3}$$

where  $N_f$  is the average number of cycles to failure of the solder joint. The number of cycles until the 63.2% cumulative failure is identical to the Weibull parameter  $\eta$ , which can be observed in Weibull distribution in Fig. 5.  $\Delta W$  and  $\Delta \gamma$  is the creep strain energy density and equivalent creep strain that changed in one cycle, respectively.  $A_1$ ,  $A_2$ ,  $n_1$  and  $n_2$  are coefficients that need to be determined by experiments. Equation (2) and (3) can also be expressed in a linear polynomial form as below.

$$\ln(N_f) = -n_1 \ln(\Delta W) + \ln(A_1); \tag{4}$$

$$\ln(N_f) = -n_2 \ln(\Delta \gamma) + \ln(A_2); \tag{5}$$

For the sake of correlating SAC105 solder joint fatigue life in a large size and low cost WLCSP, the plots for the relationship of  $\ln(N_f)$  are based on BLR TCT results as well as  $\ln(\Delta W)$  and  $\ln(\Delta \gamma)$  that come from the simulation result illustrated in Fig. 11. A linear regression trendline is added in the plot. The values of  $R^2$  is larger than 0.99 in the correlation of thermal fatigue life and creep strain energy density while equals to 0.87 in the correlation of thermal fatigue life and equivalent creep strain, which indicates that both simulation and reliability results are in a good approximation (the model with larger  $R^2$  value is being more desirable). The coefficients of  $A_1, A_2, n_1$  and  $n_2$  can be obtained through Fig. 11 as -2.2635, -3.2075, 10.226 and 1.1836, respectively. Hence, the correlated thermal fatigue life for SAC105 solder joints can be expressed as

$$N_f = 27612(\Delta W)^{-2.2635}; \tag{6}$$

$$N_f = 3.2661 (\Delta \gamma)^{-3.2075}.$$
 (7)

By using (6) and (7), the solder joint fatigue life of SAC105 in a large size and low cost WLCSP will be quickly estimated through the simulated  $\Delta W$  and  $\Delta \gamma$  in FEA without the evaluation of BLR TCT experiments.

#### IV. CONCLUSIONS

The establishment of solder joint fatigue life estimation in a large size and low cost WLCSP without a UBM layer was studied. With the good approximation for the correlation of experiments in board level reliability thermal cycling test and finite element simulations, the modified Coffin-Manson equations for SAC105 solder joint fatigue life estimation was obtained. Through the present equations, the solder joint fatigue life in a large size and low cost WLCSP can be promptly calculated by simulations without any efforts on experimental evaluations. The result is valuable and useful if high reliability and cost reduction in a large die size and low cost WLCSP are required.

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Fig. 11. Correlation of SAC105 solder joint fatigue life in a large size and low cost WLCSP (a)  $\ln(N_f)$  vs.  $\ln(\Delta W)$ ; (b)  $\ln(N_f)$  vs.  $\ln(\Delta \gamma)$ .

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