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STATS ChipPAC Ltd. 5 Yishun Street 23, Singapore 768442
***Renesas Electronics Co., 1753, Shimonumabe, Nakahara-Ku, Kawasaki, Kanagawa 211-8668, Japan**

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TSV MEOL (Mid End of Line) and Packaging Technology of Mobile 3D-IC Stacking

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seungwook.yoon@statschippac.com

Abstract

Increasing demand for advanced electronic products with a smaller form factor, superior functionality and performance with a lower overall cost has driven semiconductor industry to develop more innovative and emerging advanced packaging technologies. Memory bandwidth has become a bottleneck to mobile processor performance and lower power consumption for high performance computing needs. To reduce obstacles, a revolution in device architecture and package technologies is require. 3D TSV (Through Silicon Via) stacking is to be one of the technologies that can meet those requirements.

This paper mainly describes the 3D TSV MEOL process and packaging technology, especially TSV wafer process and thin die bonding process with Cu column bump on substrates. In order to prove the quality of this 3D package, some stress tests were conducted to evaluate the reliability on the package and board level.

The innovative TSV MEOL process and flip chip assembly with micro Cu column contributes to high density and reliable 3D/TSV integrations has been developed and demonstrated. The target package had two tier structures which consisted of a 28 nm logic device and Wide I/O memory. The logic device was fabricated by via-middle process and accompanied with over 1200 TSVs, and 40 µm / 50 µm bump pitch layout. Advanced 300mm backside via reveal (BVR) process was developed with thin wafer handling and temporary bonding/debonding process. Thermocompression bonding method with Cu pillar was applied to both connections between the memory die and the logic die and between the logic die and an organic substrate so that the high reliability could be achieved. As reliability test items, temperature cycling test, high temperature storage test, humidity test, unbiased highly accelerated stress test and pressure cooker test were performed and passed JEDEC standard reliability tests as well as board level reliability test. After functional test with stacked 3D TSV with logic and Wide IO memory, 12.8 GB/s transmission and drastic I/O power saving compared to LPDDR3 were observed.

INTRODUCTION

Moore's law is approaching physical limitations of CMOS scaling, and three dimensional (3D) integrations have been proposed as solutions [1,2]. The wide band transmission between the logic and the memory is becoming indispensable for not only mobile products, but also other products related to a network area such as servers and data centers. These days 3D integration with Through Silicon Via (TSV) is considered as the key solution, which brings benefits leading to low power consumptions and downsizing of products[3-5].

Advanced flip chip bonding process is one of the key technologies to realize 3D TSV integrations[6, 7], and to enable heterogeneous integrations which combines different functional devices (logic, memory, RF, MEMS etc.). Especially, to develop effective underfill methods for 3D is unavoidable to relieve mechanical stresses so that the reliabilities of interconnections can be enhanced [8-11].

This paper mainly describes 3D TSV packaging technology of mobile 3D-IC stacking, especially MEOL process, package assembly and it reliability. In order to prove the quality of this 3D package, component and board level reliability tests were conducted to evaluate the reliability on the package level. Finally, 28 nm logic device and Wide I/O DRAM were assembled into 3D structure for functionality demonstration with this new technology.

3D Advanced Wafer Level (WLP) Packaging Evolution

Increasing demand for more advanced, smaller and lighter mobile products with superior functionality and lower overall cost has driven the development of innovative and sophisticated packaging technologies, as shown in Figure 1. One of the exciting electronic market trends is the growing availability of mobile devices, such as smartphones, tablets and ultrabooks, which fully realize the dream of computing and communication convergence, with adequate bandwidth and speed to provide a rich user experience. It is particularly important that the next generation of WLP meets the increasing demand for higher bandwidth, improved thermal dissipation and enhanced reliability in cost-effective, scalable solutions to satisfy the growing mobile market.

The need for higher levels of integration, improved electrical performance / reduction of timing delays and shorter vertical interconnects is driving a shift from 2D to 2.5D and 3D package designs. 3D integration is proceeding on three fronts--moving from package level (die and package stacking) to wafer level (especially Fan-out WLP), and, more recently, to the silicon (Si) level with TSV and interposers. Today's new lightweight mobile computers are innovative devices providing true convergence with powerful computing functions, high speed communications and visual, sensing, and imaging technologies. This convergence is pushing traditional packaging well beyond its typical limits in the areas of form factor, reliability and performance.

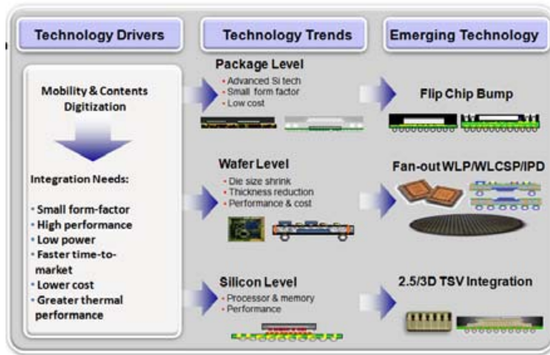

Figure 1: Emerging technology trends for the mobile marketplace.

3D TEST VEHICLE (TV) DESIGN AND DETAILS

The target 3D vehicle consisted of Wide I/O DRAM with micro-bumps, the logic device with high density TSVs and fine pitch Cu pillars and an organic substrate, as shown in Fig. 2. NCP was adopted as an underfill material to protect flip chip joints between the logic die and the substrate.

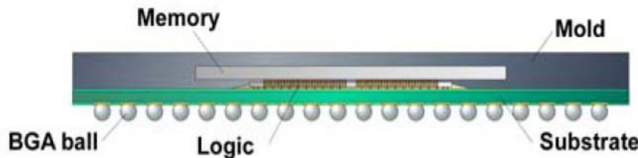

Figure 2. Schematics TSV 3D IC stacking.

Table I. Specifications of logic and memory TV

		Logic TV	Memory TV
Die size [mm]		6 x 6	9 x 9
Die thickness [um]		50	260
TSV	Diameter [um]	10	-
	Depth [um]	50	-
	Pitch [um]	40,50(x,y)	-
	Process	Via-middle	-
Front-side	Pad layout	Center, peripheral	Center
	Pad count	900	1200
	Pad pitch [urn]	100 um staggered	40,50(x,y)
Back-side	Pad layout	Center	-
	Pad count	1200	-
	Pad pitch [urn]	40,50(x,y)	-
Substrate	Thickness [mm]	0.22	
	Metal layers	4 metal layers (1/2/1 buildup substrate)	
Package	Size [mm]	14 x 14	
	Height [mm]	< 1.0	
	Structure	700 I/O BGA	

Table I summarizes major specifications of the logic TV, the memory TV and the substrate. They were designed to clarify behaviours of 3D structure in the following reliability tests. The logic TV was fabricated by so called via-middle process and accompanied with 1200 TSVs, a size of 6 x 6 mm^2, a thickness of 50µm and 40 µm/50 µm UBM pitch in x-y directions. Cu columns on the front-side were built along peripheral four rows (100 µm pitch for each row) and on the center area of the die. Solder caps of Cu pillars were formed by electroplating with SnAg. The interface between the logic and the memory was designed by following JEDEC standards. Wide I/O DRAM had 260 µm-thickness, 9 x 9 mm2 size and micro-bumps in the center area of the die. The target of total package thickness including BGA balls was less than 1.0 mm.

3D TSV MEOL PROCESS

TSV MEOL process flow occurs between the wafer fabrication and back-end assembly process. MEOL processes support the advanced manufacturing requirements of 2.5D and 3D TSV as well as wafer level packaging, flip chip and embedded die technology.

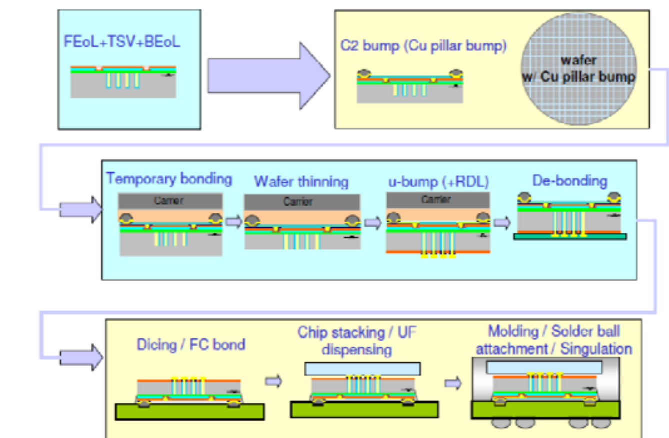

Figure 3. MEOL and package assembly steps in overall 3D TSV process flow.

Flip chip and wafer level packaging are important drivers of mid-end processing in addition to the anticipated growth in 3D solutions utilizing TSV technology, particularly with the integration of memory and logic devices at advanced technology nodes. The initial markets that are expected to embrace 3D TSV technology are mobile applications, memory stacking and high performance processors for the computing segment.

Cu COLUMN MICROBUMP PROCESS

Micro bumping technology where bump pitches are less than 50 micrometers using solder is explored extensively in industry for realization of miniaturized 3D IC integration. For Wide IO microbump in JEDEC 42.6 standards, it has 50/40um bump pitch in x/y direction, respectively. Cu column with solder cap micro-bumps have been studied with the objective to develop reliable fine pitch solder micro joints at low cost. Microbump fabrication is based on photolithography and electroplating processes, which is compatible with conventional IC fabrication. The fabrication process of wafer level process starts with bare Si wafer using Ultra Violet (UV) - light lithography of spin on dielectric material. Secondly, Redistribution line (RDL) layer plating to re-route the Al/Cu bond pads to microbump locations. Thirdly, passivation of RDL layer using spin on dielectric coating and UV

lithography to open the RDL metal pads at the bump pads. Fourthly, deposition of Ti or TiW/Cu seed layer and patterning of thick photoresist film using lithography to copper pillar plating and then Ni/solder plating. SEM micrographs of microbump are shown in Fig.4 for 20µm diameter and 40µm height microbumps for 80/40µm staggered bump pitch.

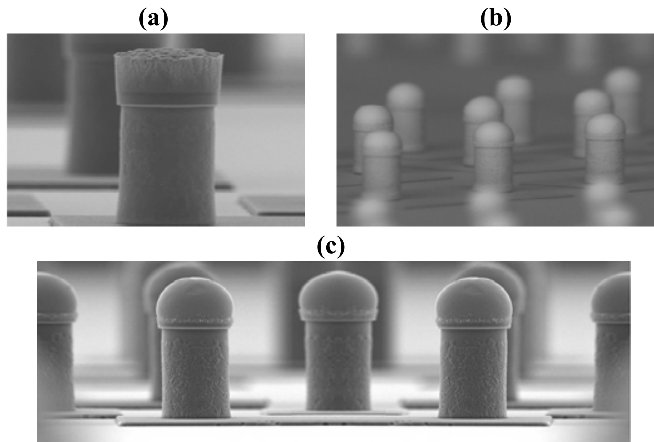

Figure 4. Micrographs of micro bump (a) after micro-bump fabrication and (b & C) after reflow

BACKSIDE VIA REVEAL (BVR) PROCESS

As shown in 3D TSV process flow of Fig.3, TSV is revealed to backside for 3D vertical interconnection after front-end TSV formation. With temporary bonding/debonding system, TSV wafer from fab is to be thin-down and Si etched to expose Cu via with fab process. TSV Cu was fully protected through high selective Si etch process to assure no Cu contamination. (Fig.5) There was also TOF SIMS (Time-of-Flight Secondary Ion Mass Spectroscopy) analysis for Cu contamination on Si wafer during CMP (Chemical Mechanical Polishing) process and verified non-detectable Cu content after chemical composition analysis along whole 300mm TSV wafer. Fig. 6 shows SEM cross-section view and photo of solid Cu filled TSV of 10um diameter and 50um depth after BVR process. Fig. 7 shows TTV (total thickness variation) of 3D TSV wafer after BVR process. It showed only a few microns of TTV values of 300mm test vehicles after process optimization with several DOEs.

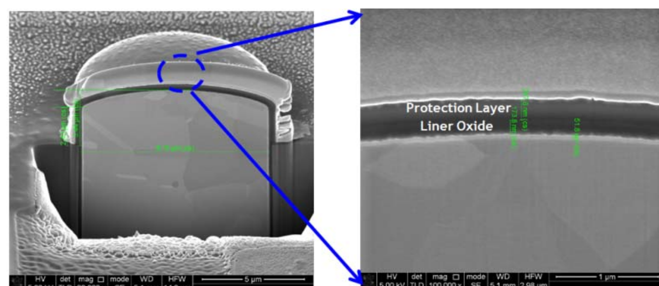

Figure 5. FIB SEM micrographs of protective Cu TSV BVR process.

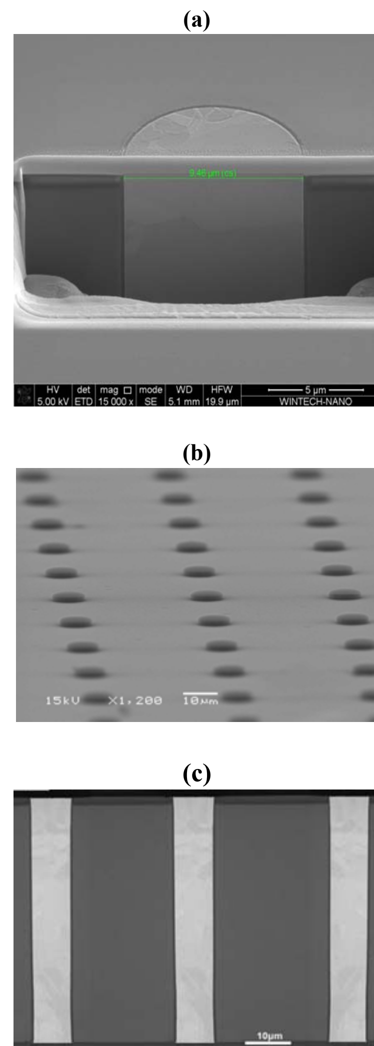

Figure 6. SEM micrographs of backside TSV via revealed after CPM and Si etching process in 12” 3D TSV wafer. (a) FIB titled view of TSV via revealed, (b) revealed Cu tips and (c) cross-sectional view of 10um diameter and 50um depth TSV

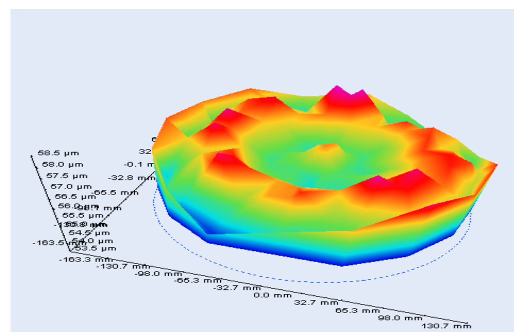

Figure 7. Total thickness variation (TTV) of revealed TSV wafer with temporary bonding.

3D TSV ASSEMBLY AND PACKAGING

Compared to conventional flipchip process, TSV assembly process is more complex due to TSV wafer as well as

microbump. As shown in Fig. 8, there are additional materials, like as additional encapsulation in between bump and flipchip die or bump and TSV die. There are quite critical challenges for assembly view point both in materials and assembly process.

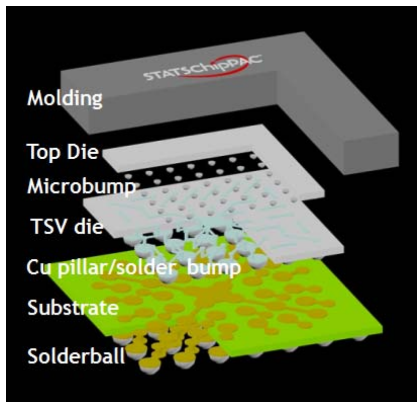

Figure 8. Schematics of TSV 3D IC packaging.

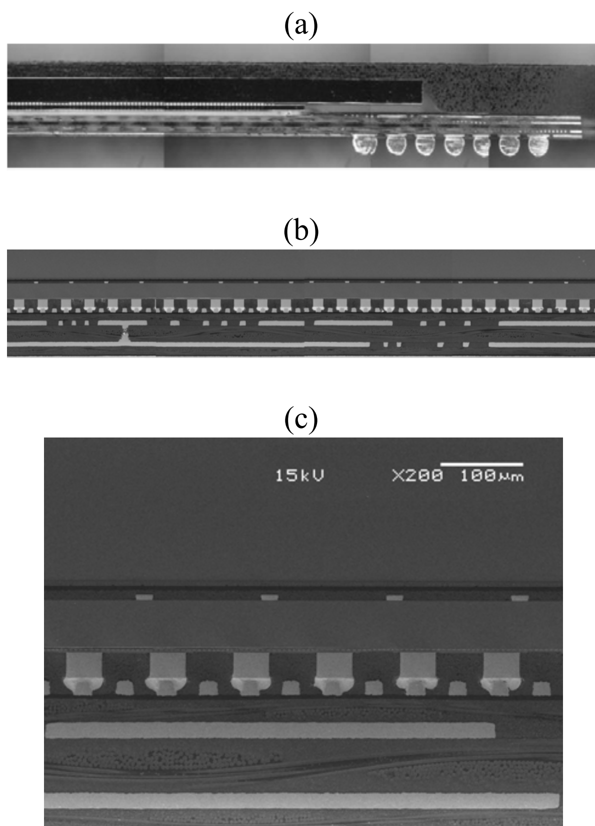

Figure 9. Micrographs of (a) cross-section of 3D IC stacking and (b,c) 40/80 µm pitch of chip-to-substrate bonding.

In advanced 3D TSV stacking technologies, one of the important steps is to develop and assembly fine pitch and high density solder microbumps. Solder microbumps for flip-chip interconnections allow high wiring density in the Si-carrier, as compared to organic or ceramic substrates, and enable high-performance signal and power connections.

Flip chip assembly was carried out to establish bonding process and investigate the reliability with Cu pillar microbump. After microbump test vehicle fabrication with bump, the flip chip attachment was carried out. Several DOE (design of experiments)s were carried out to find optimized flip chip attach process conditions as functions of time, temperature and pressure. Assessments by checking fractural surface and mechanical shear strength were conducted to evaluate DOEs of bonding parameters.

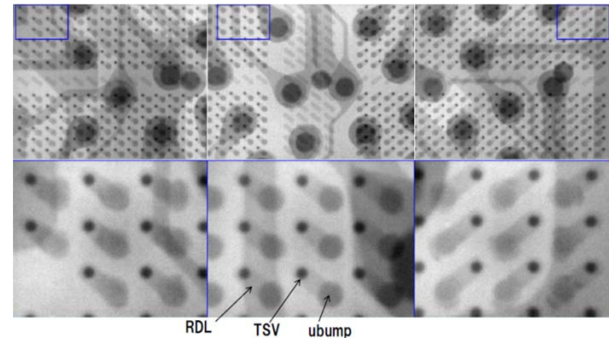

Figure 10. X-ray micrographs of 40/50µm pitch of chip-to-chip bonding of 3D TSV IC stacking

Fig. 9 shows the micrographs of cross-section of the chips joined for 40µm pitch microbumps. A misalignment of about <2µm was observed between the Si chip and 3D TSV chip after assembly. This misalignment was a result of accuracy limitation of the bonder equipment. After assembly, X-ray image was observed and found successful 3D TSV flipchip bonding without voids in between chip-to-chip, chip-to-substrate, respectively as shown Fig.10.

ELECTRICAL PERFORMANCE VALIDATION[1]

Largest benefit of 3D integration is the capability to realize System in Packages (SiP) which consist of different wafer technologies. To evaluate actual performances of the unique assembly process developed in this study, the 3D package which combined 28 nm logic and Wide I/O DRAM was assembled. This 3D package had the extremely small logic device as a bottom die and the large memory device as a top die. The logic device was fabricated with 28 nm technology, and accompanied with 1200 TSVs, a size of 2 x 6mm^2 and a thickness of 50 µm. The memory device was a 4 Gbit 512 DQs monolithic Wide I/O DRAM, and accompanied with a size of 9 x 9 mm^2 and a thickness of 260 µm. The developed assembly process could fill the space between the bottom die and the top die. After the assembly, electrical performances of the samples were evaluated with LSI testers. Not only the 1200 TSVs connectivity, but also DRAM bit quality, at speed test, current consumption were investigated carefully. In conclusion, it was proved that the test vehicle achieved 12.8 GB/s transmission and 89 % reduction of I/O power compared to LPDDR3.

COMPONENT AND BOARD LEVEL RELIABILITY

The reliability of the target 3D package was evaluated by temperature cycling (TC), high temperature storage (HTS), humidity test (HT), unbiased highly accelerated stress test (uHAST) and pressure cooker test (PCT). Table II summarizes the stress conditions and results. Before the reliability tests, all samples were treated with the moisture sensitivity level 3 (MSL3) (30°C /60% RH, 168h) and three times reflow (a peak reflow temperature: 260°C). In this test vehicle, daisy chains were laid out to evaluate the connections among the logic die, the memory die and 1200 TSVs. The resistance of each daisy chain was measured periodically in all test items. And board level reliability tests were also carried out as shown below in Table II.

In these tests, the criterion of resistance increase was decided to be within 20 % of each initial value. The resistance changes in all reliability tests were less than ± 3 %. In conclusion, all the samples passed component and board level reliability.

Table II. Test items and results of package and board level reliability tests.

Test Item (Test condition)	End point	Results
1.Component Level Test		
Temperature Cycling (TC C -55/125degC)	1500 cycles	pass
High Temperature Storage / HTS (150degC)	1000h	pass
Humidity Test /HT (85degC/85%RH)	1000h	pass
Unbiased Highly Accelerated Stress Test /uHAST (130degC/85%RH)	500 h	pass
Pressure Cooker Test/PCT (121degC/100%RH)	300h	pass
2.Board Level Test		
Temperature Cycle Test JEITA	500 cycles	pass
Mechanical Drop Test JEDEC	30 drops	pass
Cyclic Bending Test JEITA	1500 cycles	pass
Board Bending Test JEITA	-	pass
Allowable Bending Test JEITA	-	pass
Impact Bending Test JEITA	-	pass

CONCLUSION

1. The innovative assembly of 3D TSV MEOL and package assembly technology has been developed for reliable 3D/TSV integrations.
2. Cu pillar bump, temporary bonding debonding and BVR process were optimized and qualified with 300mm daisychain and 28nm functional wafers.
3. Package assembly stacking process was established for chip-to-chip, chip-to-substrate interconnection with thermocompression bonding with 40/50um ultra-fine pitch microbump.
4. All of the samples passed 1500-cycle TC, 1000h HTS, 1000h HT, 500h uHAST and 300h PCT and board level reliability including TCoB and bending tests.
5. 28 nm logic device and Wide I/O DRAM were assembled into 3D structure with this technology.
6. 3D test vehicle showed 12.8GB/s transmission and 89% reduction of I/O power consumption compared to LPDDR3. As a result, the robust process for 3D integration was established.

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