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Optimization of Compression Bonding Processing Temperature for Fine Pitch Cu-Column Flip Chip Devices

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Abstract

For the demand of high density input/output (I/O), finepitch, and low-k materials in copper column bump flip chip packages, Thermal Compression Bonding (TCB) with preapplied Non Conductive Paste (NCP) has been developed in order to ensure manufacturing reliability. The narrow bonding process window of pre-applied NCP, short bonding time, and high bonding head temperature can cause low yield issues such as NCP voiding in solder and no solder wetting on substrate. For this reason, the bonding parameters, such as bonding temperature profiles and dwell times, have to be controlled and optimized to achieve good solder wettability.

In this paper, the optimized maximum bonding temperatures and timing of the TCB process for fine pitch copper column flip chip package are examined. A thermal simulation is also conducted to correlate with experimental data. In the experiment, the bump temperature is measured with a thermocouple while the bonding head temperature and time are controlled with a heat controller. In the thermal simulation, a transient approach is used to consider the bonding temperature profiles and boundary conditions.

The paper concludes with an approach and methodology to obtain optimized bonding temperature profiles which is crucial for the development of next generation fine pitch flip chip devices.

Introduction

As the number of I/Os continues to increase in many advanced devices, semiconductor package sizes and bump pitches become smaller and silicon (Si) nodes get narrower. For the conventional flip chip bonding process, the copper and solder bumps are self-aligned in between the die and substrate in a standard reflow in the manufacturing process to achieve high production yields. However, there is a high risk of die and bump cracking in the manufacturing process, especially for advanced packaging requirements. The typical failures are bump and die cracking, and bump bridging in the underfill fill steps. One of root causes of the failures is that the traditional reflow process introduces high thermal stresses [1]. То address these kinds of issues and to simplify the manufacturing processes for the next generation of packaging, TCB provides a good solution.

Thermal Compression with Non-conductive Paste (TCNCP) is an alternative solution to improve the quality of interconnection between die and substrate. This process basically combines both capillary underfill process (CUF) and molded underfill process (MUF) into one single process. TCNCP minimizes the number of process such as fluxing, die attach, reflow, deflux, and baking, which are typically used in the conventional CUF or MUF processes. The TCNCP process is able to prevent bump bridging and die/bump

cracking as well as minimizing the voiding issue which is commonly seen in the CUF and MUF processes, especially for very small gaps in between the die and substrate.

However, the application of TCNCP requires careful thermal management. The temperature controls for the heating sources and the heat transfer from heating source to bumps must be tightly controlled in order to achieve the optimized bump temperature for the purposes of melting and soldering. To minimize voiding issues such as air entraps, a very short time window for curing has to be used in the NCP process.

The goal of this paper is to predict the temperature distribution of the copper/solder interconnection location. The temperature distribution is the key factor determining the NCP filling quality, solder shapes, adhesion strength of interconnections, and thermal stresses. Both experimental and simulation approaches are used in this study. The numerical approach provides an economic means to predict the temperature distribution to lower the manufacturing cost [2, 3].

TCNCP test vehicle

In this study, the test vehicle is a flip chip very fine Ball Grid Array (fcVFBGA). The device has 14x14x0.8mm body size and flip chip die 11x11x0.1mm. The test die is built with daisy-chain circuits for the open/short test and there are over three thousand bumps populated in the center and at the peripheral of the die. The pitch of bumps is around 80um for the central bumps and 40um for the peripheral bumps. The height of copper/solder interconnection is 42um. The substrate has 4 metal layers and Figure 1 is the schematic drawing of the test vehicle. Table 1 lists the package and substrate information.



Figure 1. Cross sectional view of the package

	ltem	Description	
DVC Ture	PKG type	FCVFBGA	
РКО Туре	PKG size	14×14mm	
Device	Die size	11×11mm	
	Die thickness	100um	
Bump	Bump Count	Over 3000	
	Bump pitch	40/80um	
	Bump height	42um	
Substrate	Туре	Strip type	
	Substrate layer	4-layer	
	Core Thickness	150um	
	Bond Pad Finish	OSP	
NCP Material		Material A	

Table 1. Package and substrate

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Advantages of TCNCP

There are a number of advantages with the TCNCP For the conventional flip chip manufacturing process. process, there are several process steps involved such as die preparation (DP), chip attach and reflow, flux cleaning or deflux, baking, underfill and underfill curing, and the molding. With the application of TCNCP, two to three processing steps may be removed as shown in the Figure 2. Before the thermal compression bonding with pre-applied NCP, the TCNCP goes through the die preparation (DP) which is the same as a conventional flip chip manufacturing process. The DP involves wafer back grinding and laser grooving which separates each die from the wafer. After the DP, the substrate in the TCNCP process is then baked to remove the moisture and prevent the voiding risks. Following the substrate baking, the substrate was cleaned with a plasma cleaning process to remove surface impurities and achieve a better surface adhesion for compression bonding and better flow of NCP materials. Figure 2 shows that with TCNCP process, the reflow and deflux steps are removed, thus the simplification and lower manufacturing cost.



Figure 2. Conventional flip chip vs. TCNCP manufacturing process

Consideration of processing parameters

From previous section, the TCNCP couples the chip attach step with underfill step to lower the manufacturing cost. The simplified process involves detailed procedures and considerations such as the bonding force, NCP dispensing, bonding tool setting, and the temperature profile as shown in the Figure 3. These four key process parameters have to be carefully controlled and monitored to obtain the best optimization. Various conditions and parameters were carefully tested at STATS ChipPAC to ensure the reliability of the final packages.

Bonding force was adjusted and selected to have a good quality of bump shape after soldering and stand-off height. If the bonding force is too high or too low, the solder cap may be squeezed too much or may have non-wetting issues. The dispensing volume, rate, and pattern of NCP were also carefully controlled to minimize the void and overflow. The bonding tools were calibrated and adjusted to ensure the test parts and machine components were accurately aligned. This step is crucial, especially for the fine pitch devices, to achieve short process time and to avoid the contamination of NCP overflow or foreign material on the bonding heads and machine tools [4, 5].



Figure 3. Key parameters for TCNCP

To have a successful bond, one of the most important keys is to obtain an optimized temperature profile which considers the ramp up/down speeds and times. The ramp up/down speeds and times affects the NCP flow behavior, void creation, and residual stress of the final product. In this regard, the peak and dwell time shall be precisely controlled to provide enough time for melting and soldering of bumps with substrate pads.

In this study, the target bonding peak temperature of the test vehicle surface was set to be 250C. In order to achieve this temperature within a short time, the temperature of bonding heads has to be heated to over 400C using rapid ramp-up speed. For the production concern, the entire process flow, which includes the NCP spreading and melting of solder, has to be controlled to within 5 seconds. Figure 4 demonstrates a schematic drawing of the temperature profile of the compression bonding steps.

(Step 1) Pick and deliver a die from wafer to the substrate and align the die with substrate which is already being dispensed with NCP material.

(Step 2) Place and mount the die on the substrate. The bottom substrate and top die have different initial temperatures, but all parts are heated rapidly as shown in the figure.

(Step 3) In this step, the parts are heated rapidly to reduce the process or cycle time. The peak temperature and the dwell time, which are for the melting of solder and the curing of NCP, have to be carefully monitored and controlled. The curing rate and time will determine if voids or air trappings occur inside the NCP. The improper temperature or time may also cause solder bleedings, abnormal bump shapes, bridging bumps, or non-wetting bumps. After this step, the NCP is partially cured.

(Step 4) After the die and substrate are bonded, the heating bonding head separates from the silicon and the temperatures in the parts start to drop rapidly. The

temperature in this step must be carefully controlled and monitored as well to avoid the bump or die cracking.



Figure 4. Thermal compression bonding steps

As mentioned in the previous four steps, the temperature profile has to be carefully monitored and controlled, otherwise, defects may occur.

Experimental setup

To monitor the temperature distribution of copper/solder interconnections, a thermocouple is used. The thermocouple is designated to be placed in positions where high density bumps are located. In this study, the thermocouple is placed inside the NCP material and at the peripheral bumping area, as shown in the Figure 5. The procedures for the preparation and measurement of thermocouple were as follows: (a) dispense NCP material on the substrate; (b) place and attach a thermocouple near the edge of die, and ensure the device is in the region where high density copper/solder interconnections are located. Figure 6 illustrates one sample of NCP coverage after the process.



X-section view

Figure 5. The placement of thermocouple to measure the temperature

After the preparation of thermocouple, the device goes through a standard TCNCP process flow which includes baking the substrate, plasma cleaning of the surfaces with Argon gas and beginning the pattern dispensing of flux and NCP materials. After this the device is moved to the bonding stage and the substrate was pre-heated on the stage.



Figure 6. NCP coverage after process

Figure 7 below illustrates an example of the measured temperature profile near the copper/solder The optimized temperature profile is interconnections. obtained through various experiments. The performance of each temperature profile is verified by the quality of final processed devices.



Optimization of temperature profile with simulation

Besides the experimental approach, a numerical simulation is conducted to correlate with experimental data. The simulation provides an advantage to obtain numerous data points under different conditions without the need to do all experimental legs. In this study, the focus was on the temperature prediction near the die edge in order to have an optimized temperature profile. A transient thermal simulation was conducted to study the temperature response of interconnection and the detailed simulation approaches are introduced below.

(i) Configuration of the system and boundary conditions

For this system level thermal simulation, the ambient temperature was set to be 25C and a convective heat transfer coefficient of 6W/mK was applied on the outer surfaces of the bonding machine tools. The bonding machine tools comprise the components of heater, head, and stage, as shown in Figure 8. The heater and head are made of ceramic material to sustain the high temperature application. The detailed structures and dimensions of the components are considered in the simulation.

(ii) Configuration of the package and material properties of the components

In order to accurately predict the temperatures of the copper/solder interconnections, the detailed features of the substrate were considered. The effective material properties were considered in order to determine the temperature responses of the device. Table 2 shows the material properties of the components used in the simulation.



Figure 8. System level thermal modeling

	Item	Material name	Thermal conductivity (W/mK)	Density (g/cm3)	Specific heat (J/Kg-K)
TC Bonding	Heater & Stage	Ceramic A	150	3.31	880
	Head	Ceramic B	90	3.2	670
Package	Substrate	Dielectric	0.3	1.2	880
	NCP	Material A	0.85	1.57	930
	Cu pillar	Copper	401	8.94	385
	Solder	SnAg	73.52	7.34	227
	Die	Silicon	117.5	2.34	700

Table 2. Material properties of the components

The focus of the current simulation was to predict the temperature responses of the copper/solder interconnections. Thus the distribution of copper/solder interconnection was calculated. In this study, the test vehicle package had more than 3000 copper/solder interconnections and the copper/solder interconnections with four different scenarios was considered, as shown in Figure 9.

(Option 1)

Smear all components and all substrate layers into one single material and one single layer. For this case, there was only one effective material property.

(Option 2)

Smear top copper column and top NCP as one layer, and smear bottom solder and bottom NCP as another layer. For this case, there were two effective material properties corresponding to these separate layers.

(Option 3)

Smear the internal copper/solder interconnections and internal NCP as one region, and smear the outer square of copper/solder interconnections and NCP material as another region. Outside of these two regions was the pure NCP material. For this case, the localized effective material properties were used inside each region.

(Option 4)

Simulation software was then used to import the detailed distribution of the copper/solder interconnections. For this approach, all the layers and components were captured into the simulation, thus, the material property will be position dependent. The drawback of this approach was the computational resources and time required because of the significant amount of numerical meshes.



Figure 9. Consideration of copper/solder interconnections with four scenarios

Table 3 shows the calculated effective thermal conductivities of the scenarios used in the simulation. From this table it is evident that the peripheral region of option C has a much higher thermal conductivity due to the high density distribution of copper/solder interconnections.

Option	Composition	Thermal conductivity (W/mK)	Density (g/cm3)	Specific heat (J/kgK)
1	Cu+SnAg+NCP	4.18	1.59	986
2	Cu+NCP	5.83	1.56	1030
	SnAg+NCP	1.75	1.64	921
3	Center area	3.41	1.58	973
	Peripheral area	21.87	1.70	1282
	No bumps(NCP)	0.85	1.57	930
4	Position dependent	Position dependent		

Table 3. Effective material properties

Correlation of simulation and experimental data

Figure 10 illustrates the temperature setting at the heater, the experimental measured temperatures at the peripheral NCP and copper/solder interconnections, and the simulated temperature data using four different options as mentioned in previous section. The temperature profile from the heater was calculated based on heater's ramp-up heating rate, dwell time, and the ramp-down cooling rate. The temperature profile was obtained through various optimization tests. The measured and simulated temperature distribution may be roughly divided into three zones, namely contact zone, rise zone, and drop zone. The contact zone refers to the heater and die that are in contact with the substrate. The rise zone is the temperature rising after the parts are in contact with each other and the heater is rapidly powered. The drop zone refers to the separation of heater from the device. In the simulation, the transient boundary conditions of the heater and head were considered, and a temperature monitoring point was set at the corner peripheral ring position which is the same location as the actual thermocouple.



Figure 10. Simulation result and experimental data

Figure 11 shows the experimental and simulated temperatures of the peripheral copper/solder interconnections as a function of time near their peak temperatures. Options 1 and 2, which do not consider the localized high density copper/solder distribution, have lower peak temperatures. If the simulated temperatures and the times are used in the real process, they may not be enough to melt the solder. For options 3 and 4, the peak temperatures are closer to experimental data and this is due to the consideration of localized high density copper/solder distributions.

Figures 10 and 11 predict the temperature distribution of interconnections as a function of time during the TCNCP process. The combination of the experimental and simulation approaches provide a methodology to optimize the TCNCP volume manufacturing process.

Conclusions

Following are the conclusions of this study:

- (1) Through experiment, which includes various adjustments of the manufacturing parameters and processing optimization, end-of-line fcVFBGA devices have very high yields and the defects are minimized.
- (2) The temperature control to bond the silicon, NCP material, and substrate is one of the key parameters to obtain defect-free devices.
- (3) A thermocouple was used to monitor the temperatures of NCP and copper/solder interconnections, and the temperature was compared

with numerical simulation. The experimental and simulation data were very close to each other.



Figure 11. Experimental and simulated peak temperatures

- (4) A transient thermal simulation was conducted to predict the transient temperature distribution near copper and solder interconnections. The copper trace and via on the substrate were modeled with four different scenarios. The simulation scenarios which do not consider the localized copper/solder density lead to lower peak temperatures when compared with real experiment.
- (5) The combination of the experimental and simulation approaches provide a methodology for the optimization of NCTCP process.

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